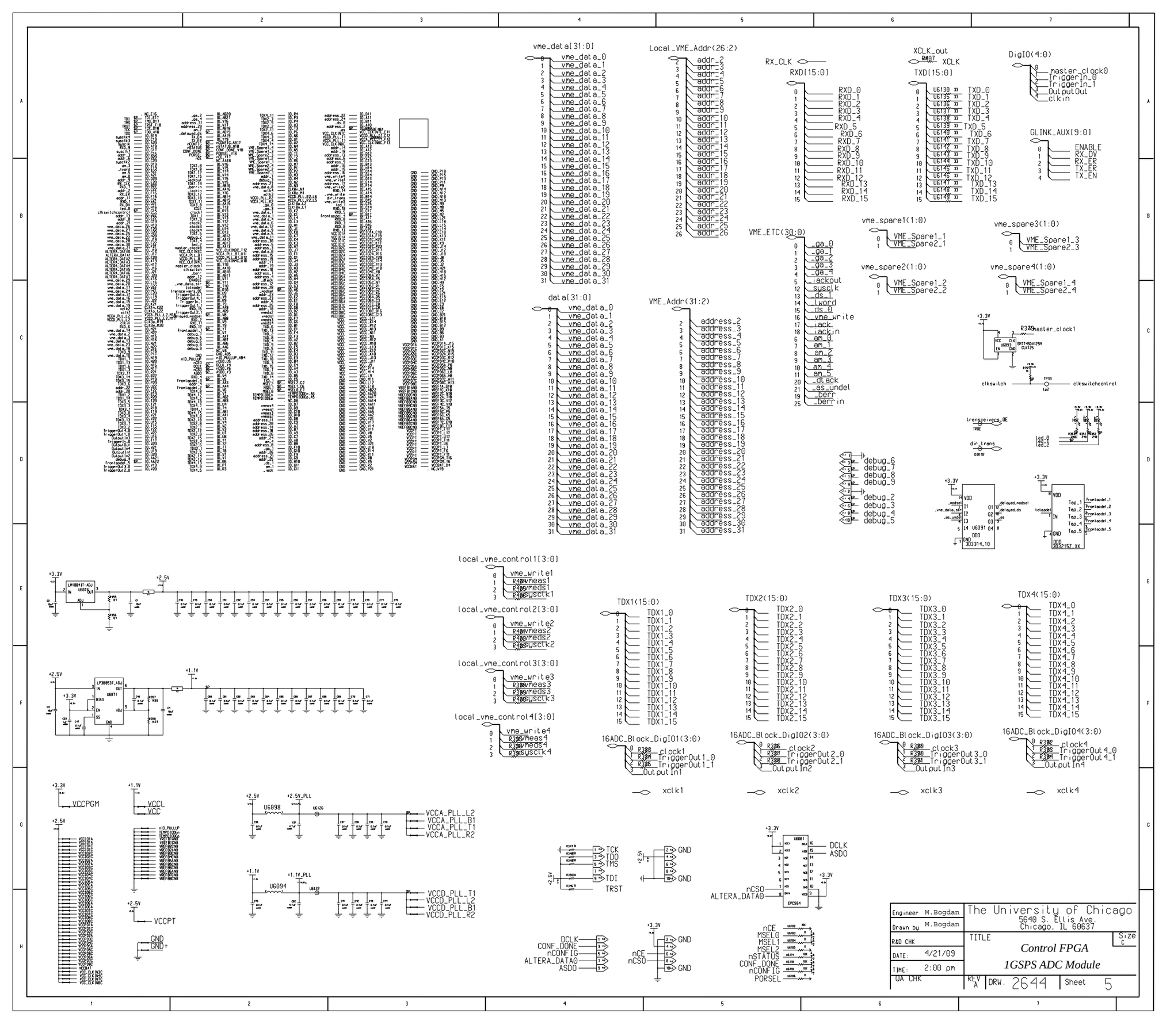
vme_data[31:0]
Local_VME_Addr(26:2)
RX_CLK
RXD[15:0]
XCLK_out
XCLK
TXD[15:0]
DigIO(4:0)
GLINK_AUX[9:0]
VME_ETC(30:0)
vme_spare1(1:0)
vme_spare2(1:0)
vme_spare3(1:0)
vme_spare4(1:0)
data[31:0]
VME_Addr(31:2)
local_vme_control1[3:0]
local_vme_control2[3:0]
local_vme_control3[3:0]
local_vme_control4[3:0]
TDX1(15:0)
TDX2(15:0)
TDX3(15:0)
TDX4(15:0)
16ADC_Block_DigIO1(3:0)
16ADC_Block_DigIO2(3:0)
16ADC_Block_DigIO3(3:0)
16ADC_Block_DigIO4(3:0)
xclk1
xclk2
xclk3
xclk4
VCCPGM
VCCPT
GND
TCK
TDO
TMS
TDI
TRST
DCLK
ASDO
nCSO
ALTERA_DATA0
nCONFIG
nCONFIG_DONE
nCE
MSEL0
MSEL1
MSEL2
nSTATUS
PORSEL
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 4/21/09
TIME: 2:00 pm
QA CHK
TITLE
Control FPGA
1GSPS ADC Module
Size C
REV A
DRW. 2644
Sheet 5