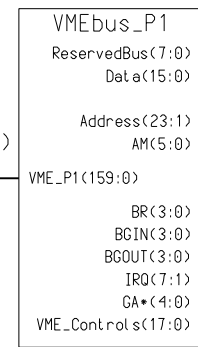


Sheet 8.1



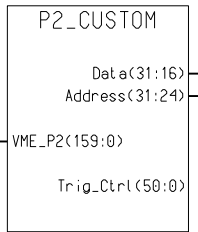
VME_P1(159:0)

DigOut(31:0)

VME_P0(94:0)

TBUSOUT(3:0)

Sheet 8.2

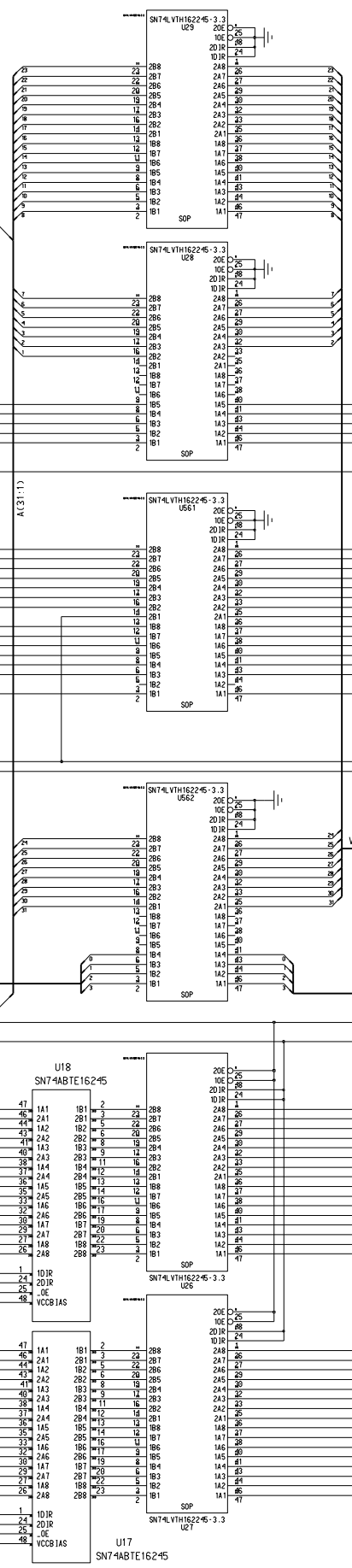


VME_P2(159:0)

TBUS_IN(3:0)

VME_P2(159:0)

D(31:0)



VME_etc(30:0)

VME_Addr(31:2)

TBUSIN(3:0)
VME_OE
VME_DIR_TRANS
Local_VME_Data(31:0)

Engineer	M. Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M. Bogdan	TITLE	Size c
R&D CHK		VME Interface 1 GSPS ADC Module	
DATE:	4/21/09		
TIME:	2:00 pm	REV A	DRW. 2644
QA CHK		Sheet 8	