

**Digital Input**  
 DigIn<15:0>  
**LVDS Repeater**  
 1 x FIN1104  
 Sheet 3

**3 Ch LVDS** →  
 ← **1 Ch LVDS**

**LVDS Repeaters**  
 4 x FIN1104  
 I01<7:0>  
 I02<7:0>  
 I03<7:0>  
 I04<7:0>  
**I/O** Sheet 4

← **4 x 3 Ch LVDS**

**LVDS Repeaters**  
 4 x FIN1104  
 I01<7:0>  
 I02<7:0>  
 I03<7:0>  
 I04<7:0>  
**I/O** Sheet 4

← **4 x 3 Ch LVDS**

**4 x 1 Ch LVDS** →

**Power**  
 +5V  
 +12Vin  
 +1.2V  
 +1.8V  
 +2.5V  
 +3.3Vin  
 -12Vin  
 GND  
 Sheet 12

**FPGA**  
**EP2S60F1020** Sheet 7

DigIn<15:0>  
 DigIn<15:0>  
 Bus\_I00<7:0>  
 Bus\_I01<7:0>  
 Bus\_I02<7:0>  
 Bus\_I03<7:0>  
 Bus\_I04<7:0>  
 Bus\_I05<7:0>  
 Bus\_I06<7:0>  
 Bus\_I07<7:0>

VME\_ETC<30:0>  
 VME\_Addr<31:2>  
 transceivers\_OE  
 dir\_trans  
 vne\_data<31:0>  
 TBUSIN<3:0>  
 TBUSOUT<3:0>  
 DigOut<31:0>  
 DigOutSer<7:0>  
 Reconfig<1:0>  
 GLINK\_AUX<9:0>  
 TXD<15:0>  
 RXD<15:0>  
 XCLK  
 RX\_CLK  
 HGLINK\_AUX<9:0>  
 HTXD<15:0>  
 HRXD<15:0>  
 HXCLK  
 HRX\_CLK

**Sheet 8**  
 VME\_ETC<30:0>  
 VME\_Addr<31:2>  
 VME\_OE  
 VME\_DIR\_TRANS  
 Local\_VME\_Data<31:0>  
 TBUSIN<3:0>  
 TBUSOUT<3:0>  
 DigOut<31:0>  
 Reconfig<1:0>  
**VME\_Interface**

P0<94:0>  
 P1<159:0>  
 P2<159:0>

**Interface**  
 Sheet 0  
 GLINK\_AUX<9:0>  
 TXD<15:0>  
 RXD<15:0>  
 XCLK  
 RX\_CLK  
 NULL

**Interface**  
 Sheet 0  
 GLINK\_AUX<9:0>  
 TXD<15:0>  
 RXD<15:0>  
 XCLK  
 RX\_CLK  
 NULL

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