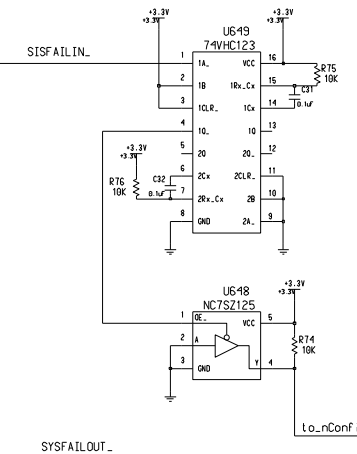
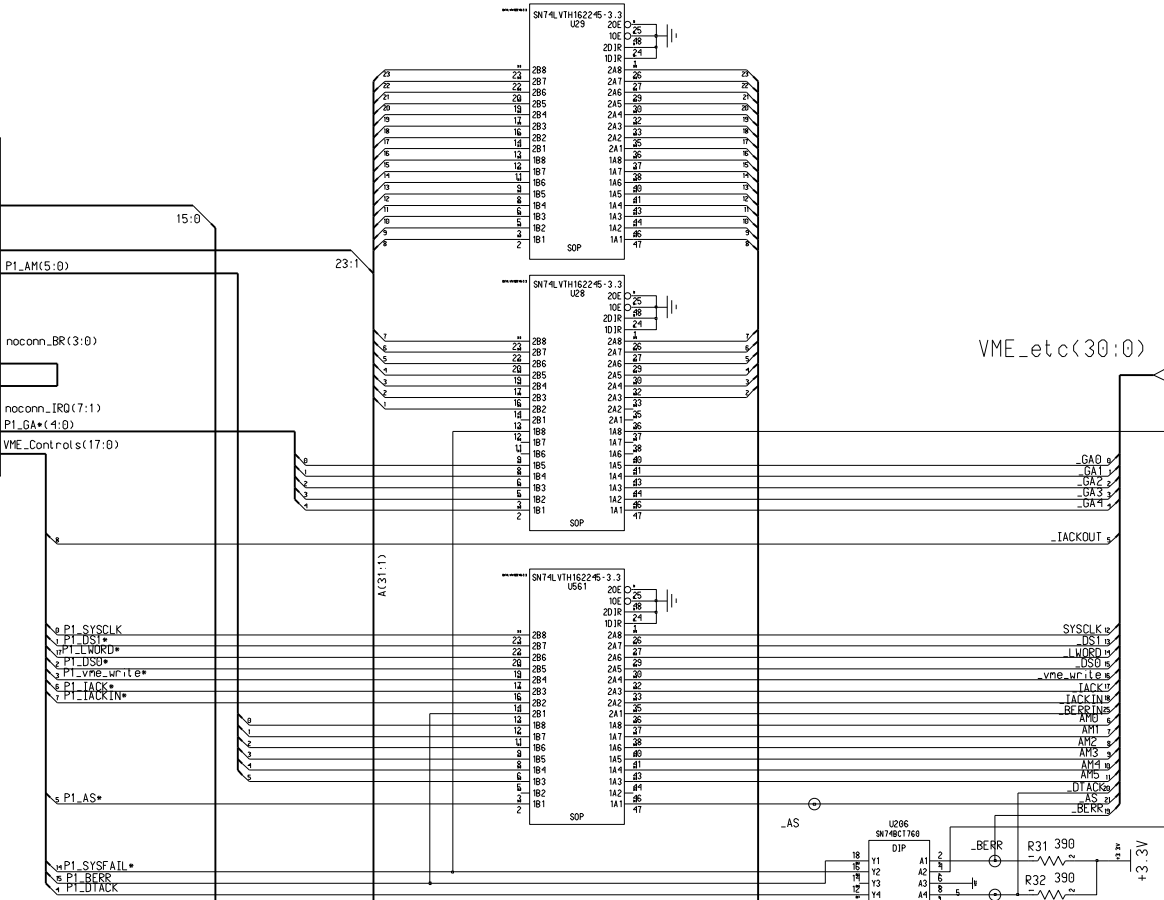
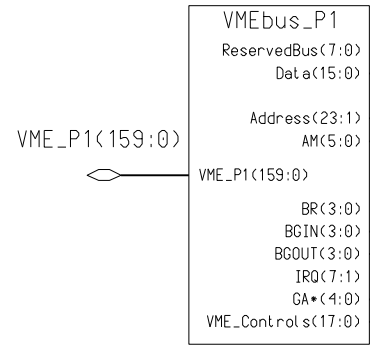
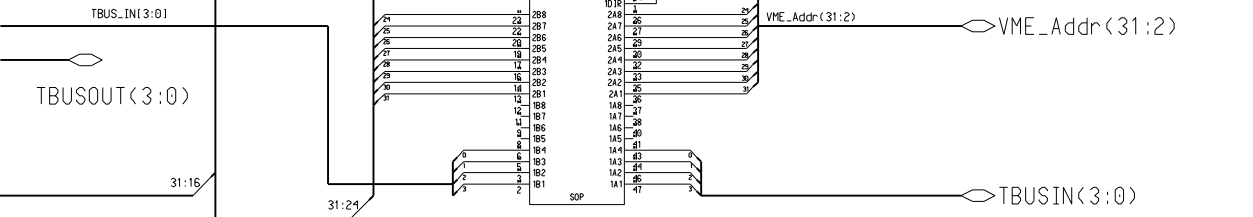
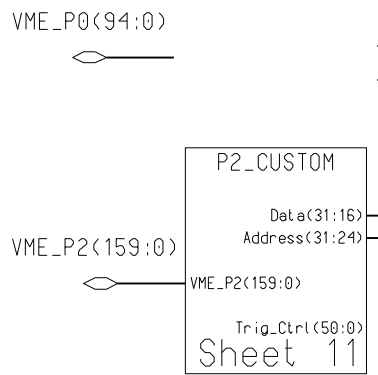


Sheet 9

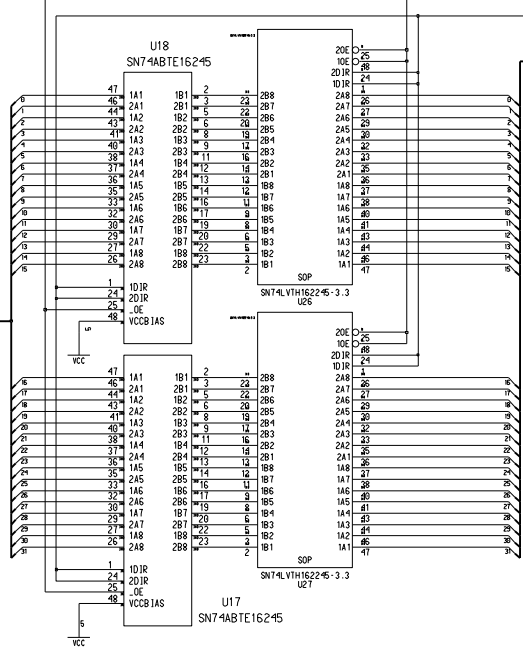


Reconfig(1:0)

Sheet 10



D(31:0)



DigOut(31:0)

Engineer	M. Bogdan	The University of Chicago	
Drawn by	M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637	
R&D CHK		TITLE	Size C
DATE:	9/16/09	VME Interface ADC Master	
TIME:	2:00 pm		
QA CHK		REV	DRW. 2655
		Sheet 8 of 12	