Sheet 9

VME_P1(159:0)

VMEbus_P1
ReservedBus(7:0)
Data(15:0)
Address(23:1)
AM(5:0)
VME_P1(159:0)
BR(3:0)
BGIN(3:0)
BGOUT(3:0)
IRQ(7:1)
GA*(4:0)
VME_Controls(17:0)

15:0
23:1
P1_AM(5:0)
noconn_BR(3:0)
noconn_IRQ(7:1)
P1_GA*(4:0)
VME_Controls(17:0)

A(31:1)

P1_SYSCLK
P1_DS1*
P1_LWORD*
P1_DS0*
P1_vme_write*
P1_IACK*
P1_IACKIN*
P1_AS*
P1_SYSFAIL*
P1_BERR
P1_DTACK

SN74LVTH162245-3.3 U29
SN74LVTH162245-3.3 U28
SN74LVTH162245-3.3 U561
SN74LVTH162245-3.3 U562
SOP

VME_etc(30:0)

_GA0 _GA1 _GA2 _GA3 _GA4
_IACKOUT
SYSCLK _DS1 _LWORD _DS0 _vme_write _IACK _IACKIN _BERRIN AM0 AM1 AM2 AM3 AM4 AM5 _DTACK AS _BERR

_AS
_BERR
_DTACK
U206 SN74BCT760 DIP NULL
R31 390
R32 390
+3.3V

SISFAILIN_
U649 74VHC123
R75 10K
C31 0.1uF
R76 10K
C32 0.1uF
U648 NC7SZ125
R74 10K
R77 0
to_nConfig
SYSFAILOUT_
Reconfig(1:0)

Sheet 10

VME_P0(94:0)

TBUS_IN[3:0]
TBUSOUT(3:0)

VME_Addr(31:2)
VME_Addr(31:2)

P2_CUSTOM
Data(31:16)
Address(31:24)
VME_P2(159:0)
Trig_Ctrl(50:0)
Sheet 11

31:16
31:24

TBUSIN(3:0)
VME_OE
VME_DIR_TRANS
Local_VME_Data(31:0)

U18 SN74ABTE16245
U17 SN74ABTE16245
SN74LVTH162245-3.3 U26
SN74LVTH162245-3.3 U27
1DIR 2DIR _OE VCCBIAS
VCC

D(31:0)

DigOut(31:0)

Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by M.Bogdan		
R&D CHK	TITLE VME Interface *ADC Master*	Size C
DATE: 9/16/09		
TIME: 2:00 pm		
QA CHK	REV A	DRW. 2655
		Sheet 8 of 12