The QUIET ADC Implementation

The ADC Board–Layout

The Q-ADC Board

Digital Output
8 LVDS Channels

Digital Output
32 LVDS Channels

Digital Input
4 LVDS Channels

Analog Input
32 diff channels

FPGA

A/D
32 channels

VME-P1

VME-P0

VME-P2

COMPONENT SIDE SILKSCREEN
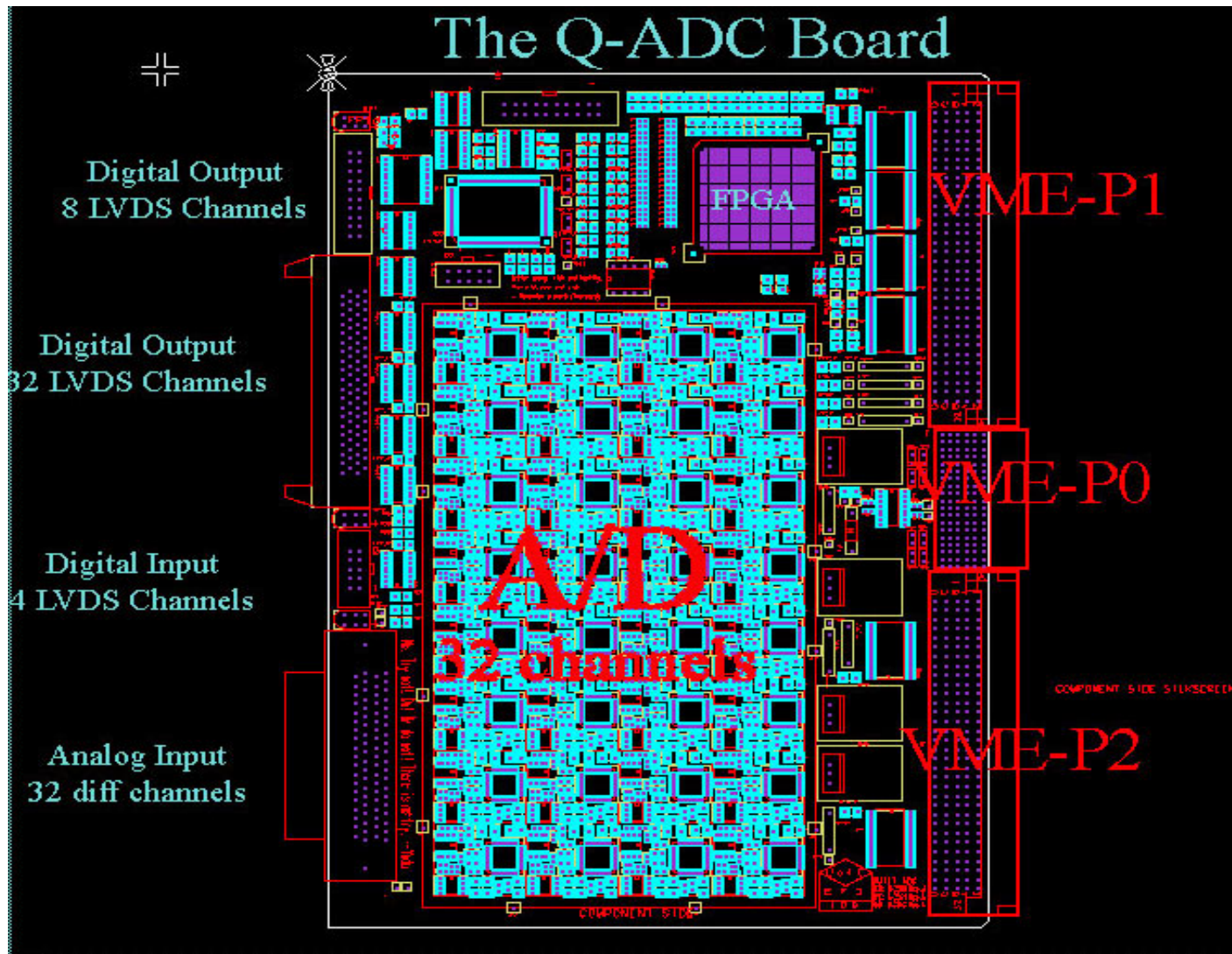
The ADC Board– Specifications

•6U VME/VIPA Board with P0,P1 and P2;

•The module is a VIPA A32/D32 slave; CBLT capable;

•Power requirements from the backplane: +5V/5A;+3.3V/5A;+/-12V/0.5A;

Front Panel connections:

•Digital Output 1: 32 LVDS outputs on an 80-pin Honda connector. These outputs connect to the FPGA on board and are programmable via firmware change.

•Digital Output2: 8 LVDS outputs on a 20-pin header. These outputs connect to the FPGA on board and are programmable via firmware change.

•Digital Input: 4 LVDS inputs on a 10-pin header. Go to the FPGA; not used yet.

•Analog Inputs: 32 differential signals: 4Vpp (between +/- 2V).

Brief description

•Each analog input signal goes to a buffer (Gain=-1; Zi=500Ohm), implemented with a AD8022AR in a typical inverter configuration. The DC level is shifted from (-2V…+2V) to (+0.25V…+4.25V) and applied to the ADC chip AD7674.

•The AD7674 has 18-bit resolution, works in Warp slave mode at 800kSPS, with serial data reading of previous conversion during convert.

•Each ADC Channel connects independently to the FPGA (EP1S30F780C6).

•Communication between boards, for simultaneous sampling and data processing is to be done via four PECL backplane lines in P0.

•None of the Front Panel digital I/O lines is configured yet.