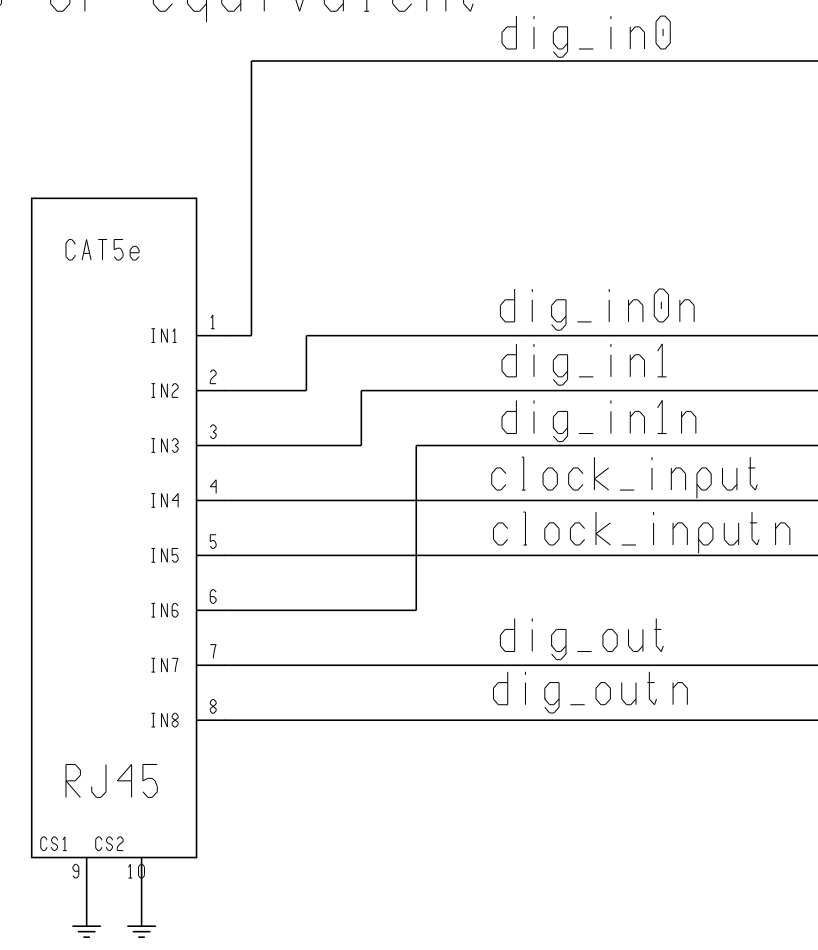
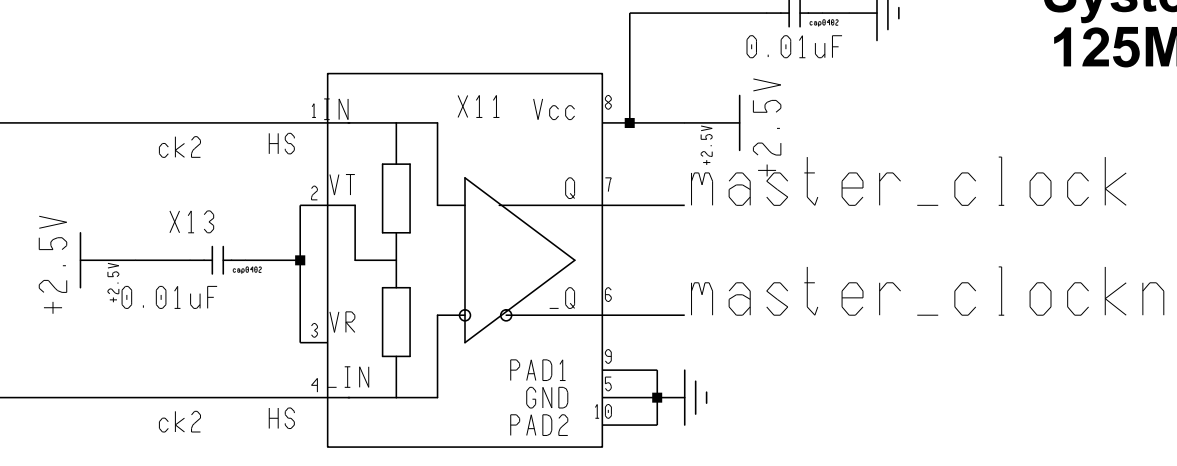
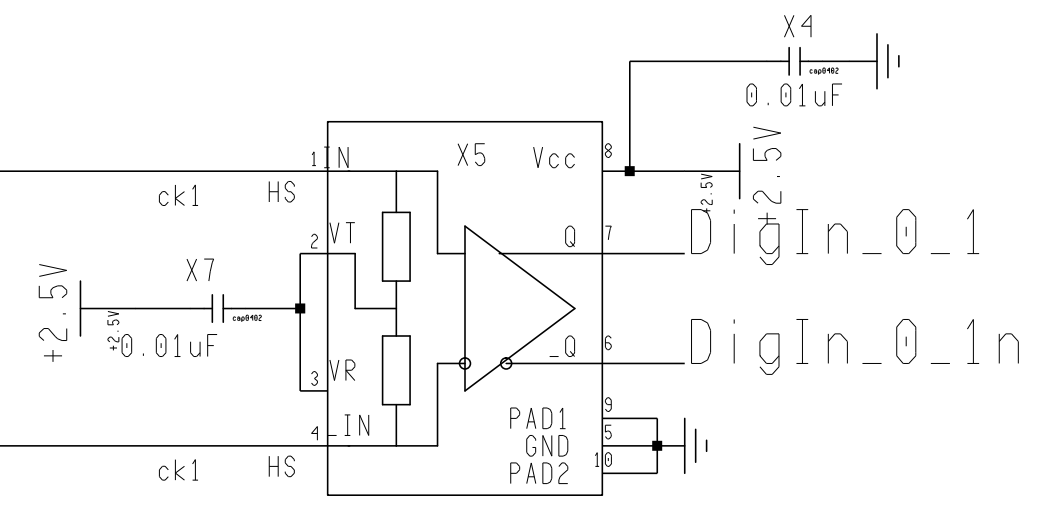
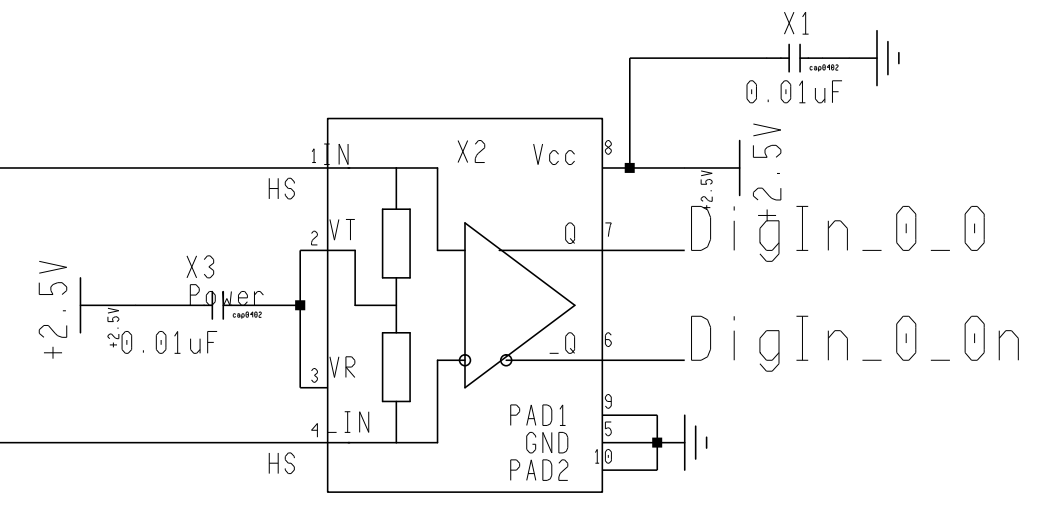
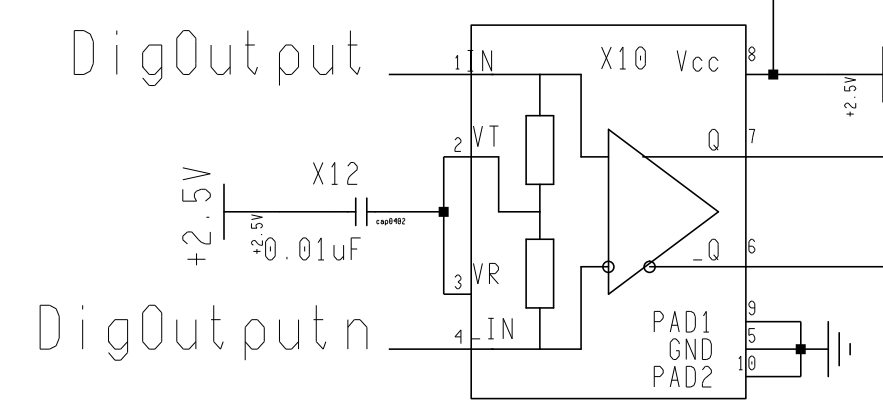


RJ45 Connector
AJT65B8813 or equivalent



SY58605U
LVDS Buffer

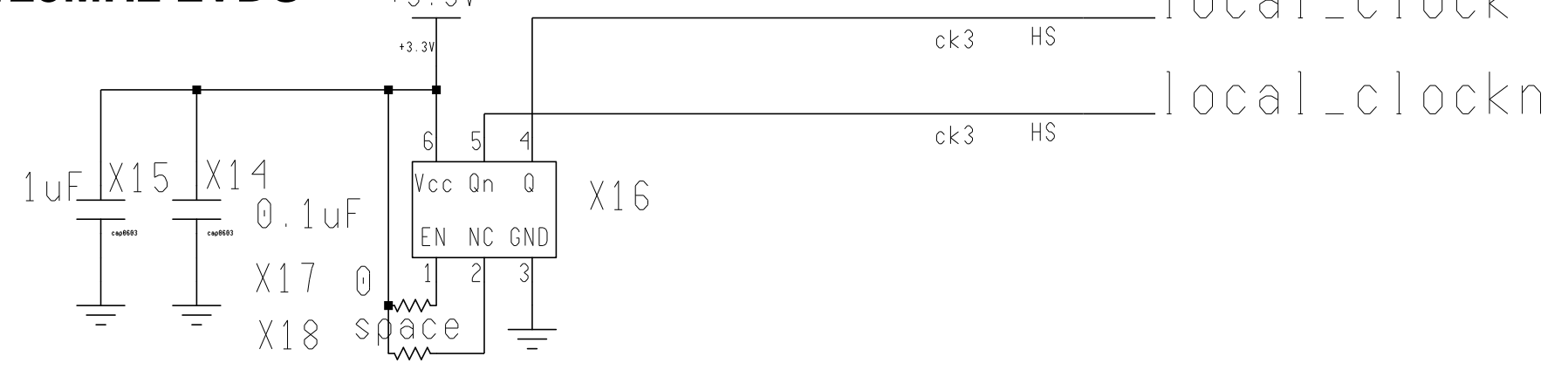


System Reference Clock
125MHz LVDS

- 0 HS DigIn_0_0
- 1 HS DigIn_0_0n
- 2 HS DigIn_0_1
- 3 HS DigIn_0_1n
- 4 HS DigOutput
- 5 HS DigOutputn
- 6 HS master_clock
- 7 HS master_clockn
- 8 HS local_clock
- 9 HS local_clockn
- 10 HS SFPclk0
- 11 HS SFPclk0n
- 12 HS SFPclk1
- 13 HS SFPclk1n

ECS-LVDS33-1250-BN

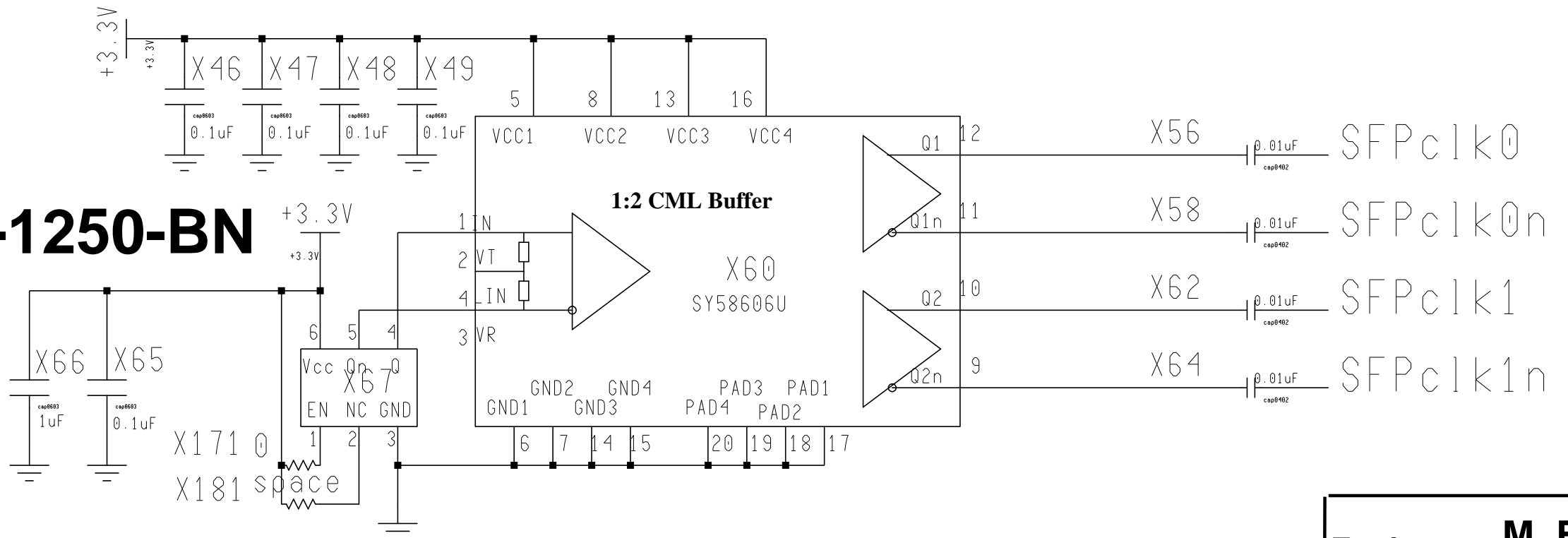
125MHz LVDS



Internal Reference Clock
125MHz LVDS

ECS-LVDS33-1250-BN

125MHz LVDS



SFP Reference Clocks
125MHz CML

Engineer: M. Bogdan	The University of Chicago Digital Input and Clocks Annie's Central Card		
Drawn by: M. Bogdan			
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