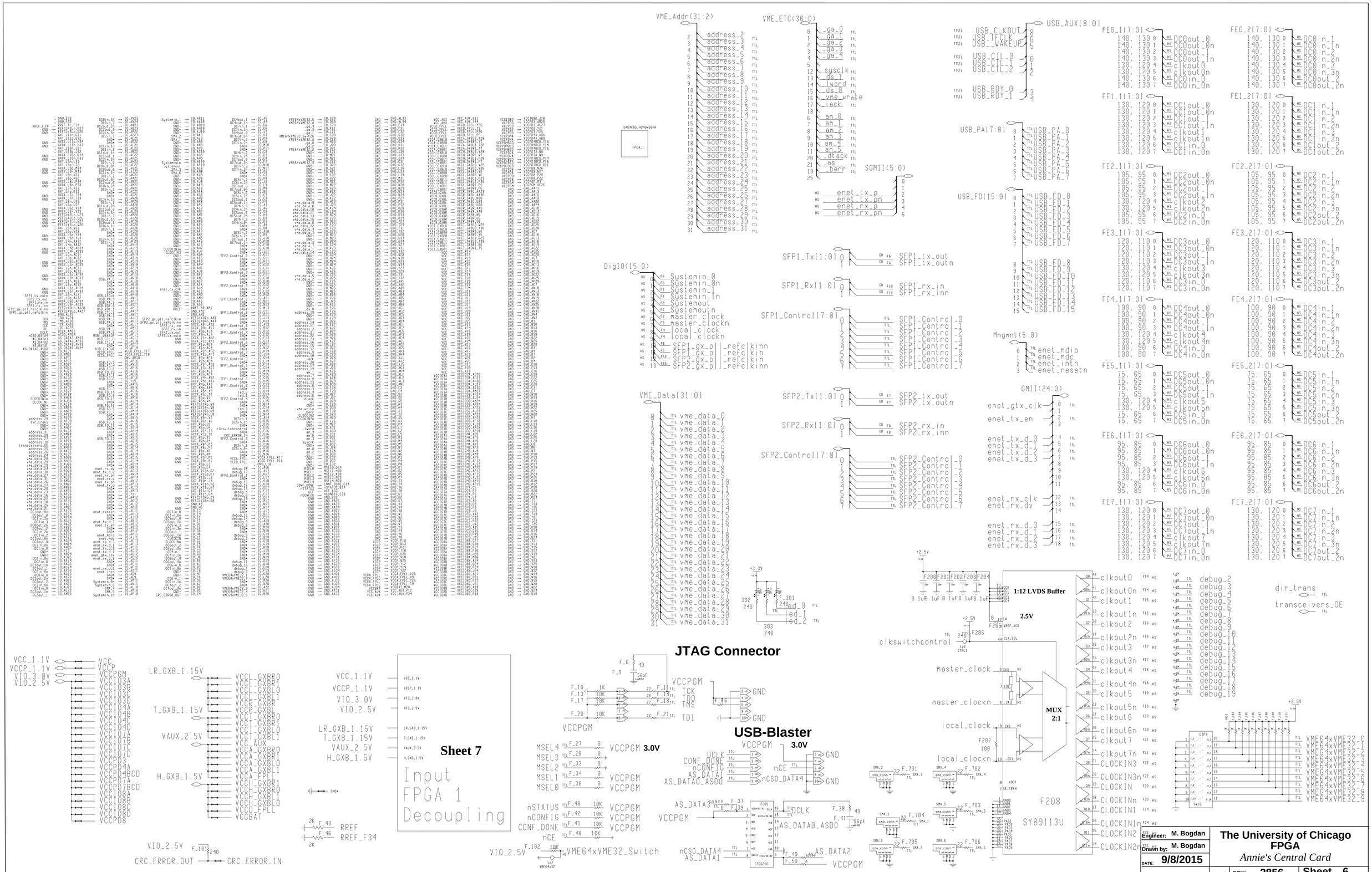
VME_Addr(31:2)
VME_ETC(30_0)
USB_AUX(8:0)
FE0_1(7:0)
FE0_2(7:0)
FE1_1(7:0)
FE1_2(7:0)
USB_PA(7:0)
FE2_1(7:0)
FE2_2(7:0)
USB_FD(15:0)
FE3_1(7:0)
FE3_2(7:0)
FE4_1(7:0)
FE4_2(7:0)
FE5_1(7:0)
FE5_2(7:0)
FE6_1(7:0)
FE6_2(7:0)
FE7_1(7:0)
FE7_2(7:0)
SGMII(5:0)
Mngmnt(5:0)
GMII(24:0)
SAGXFB5_HS40x68mm
FPGA_1
DigIO(15:0)
SFP1_Tx[1:0]
SFP1_Rx[1:0]
SFP1_Control[7:0]
SFP2_Tx[1:0]
SFP2_Rx[1:0]
SFP2_Control[7:0]
VME_Data[31:0]
JTAG Connector
1:12 LVDS Buffer
2.5V
MUX
2:1
F208
SY89113U
clkswitchcontrol
master_clock
master_clockn
local_clock
local_clockn
dir_trans
transceivers_OE
VCC_1.1V
VCCP_1.1V
VIO_3.0V
VIO_2.5V
LR_GXB_1.15V
T_GXB_1.15V
VAUX_2.5V
H_GXB_1.5V
VCCPGM
VCCPGM 3.0V
USB-Blaster
VME64xVME32_Switch
CRC_ERROR_OUT
CRC_ERROR_IN
Sheet 7
Input
FPGA 1
Decoupling
Engineer: M. Bogdan
Drawn by: M. Bogdan
DATE: 9/8/2015
The University of Chicago
FPGA
Annie's Central Card
REV. A
DRW. 2856
Sheet 6