2. Minimum trace width: 0.006" and clearance: 0.005" on Signal 1, 6 (Top and Bottom).
3. Minimum trace width and clearance: 0.005" on Signal 2, 3, 4, 5, 7, 8, 9, 10, 11, 12 (all stripline).
4. 1 oz copper for all power layers and for Signal 1, 2 (Top and Bottom).
5. Electroless Nickel Immersion Gold plating, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
6. Board Thickness: 0.093 +/- 0.008
7. Will the Top and Bottom of board on the solder side to a remaining thickness of 0.063 +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.033 unless specified otherwise.
11. Interlayer spacing as specified.
12. Zc=50 Ohm, Zd=100 Ohm for all 0.005" stripline and all 0.006" microstrip traces.
13. Via Fill and Overplate:
   - Vias of this diameter must be completely filled with Peters PP-2795 or equivalent, planarized, and plated over with Copper and surface finish.
   - The plated cap must adhere to fill material after 1x 550F solder shock.
14. Remove all non-functional inner layer pads for pins and vias.
15. Do not increase size of thermal pads and associated spoke connections on holes.

Top - Comp.Side

Layer Order
1. Signal_1, Top
2. Power
3. Signal_2
4. Power
5. Signal_3
6. Power
7. Signal_4
8. Power
9. Power
10. Signal_5
11. Power
12. Signal_6
13. Power
14. Signal_8
15. Power
16. Signal_6, Bottom

Board Characteristics - 16 LAYER BOARD:

2. Minimum trace width: 0.006" and clearance: 0.005" on Signal 1, 6 (Top and Bottom).
3. Minimum trace width and clearance: 0.005" on Signal 2, 3, 4, 5, 7, 8, 9, 10, 11, 12 (all stripline).
4. 1 oz copper for all power layers and for Signal 1, 2 (Top and Bottom).
5. 1/2 oz copper for Stripline trace layers (Signal_2, 3, 4, 5, 7, 10, 11, 12).
6. 1 oz copper for Stripline trace layers (Signal_2, 3, 4, 5, 7, 10, 11, 12).
7. Silk Screen over all signal layers.
8. Silk screen over all signal layers.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.033 unless specified otherwise.
11. Interlayer spacing as specified.
12. Zc=50 Ohm, Zd=100 Ohm for all 0.005" stripline and all 0.006" microstrip traces.
13. Present TDR test results for all signal layers.
14. Remove all non-functional inner layer pads for pins and vias.
15. Do not increase size of thermal pads and associated spoke connections on holes.