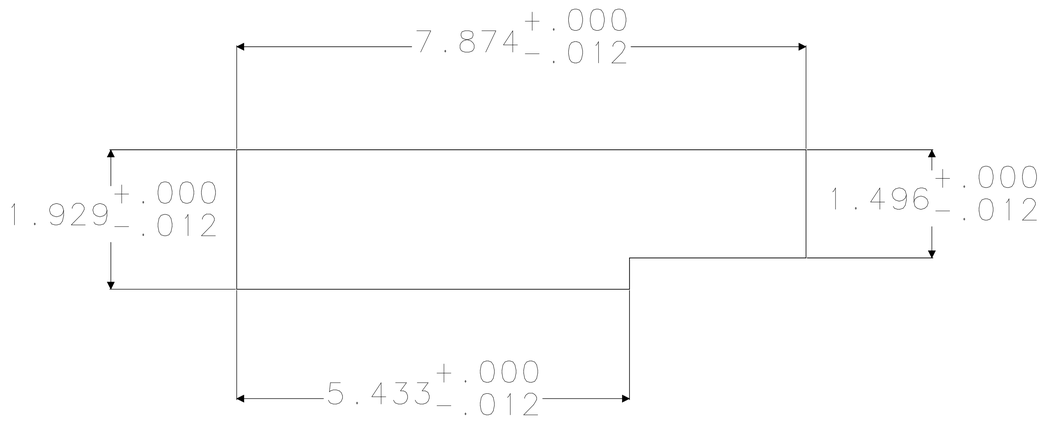

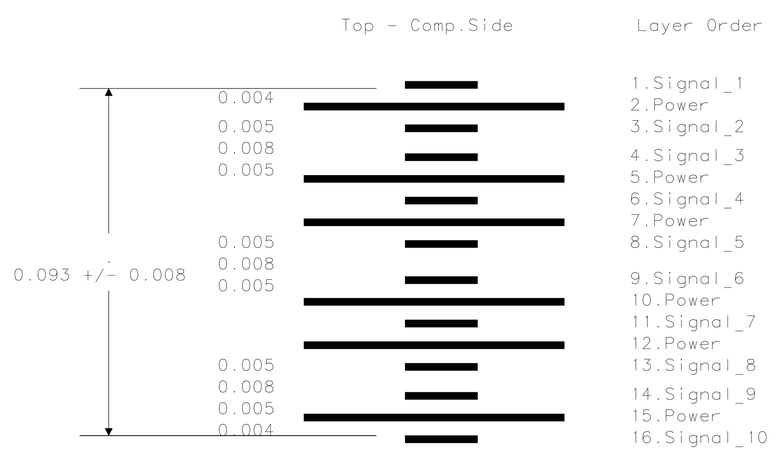

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
2. Minimum trace width: 0.005" and clearence: 0.004" on Signal Layers
3. This PCB had blind vias, and via-in-pad (VIPPO).
4. 1 oz copper for all power layers and for Signal_1 and 10 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5,67,8,9).

5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008

8. Silkscreen on Component and Solder Sides.

10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified

12. Zc=55 Ohm +/- 5 Ohm for 0.005" traces
    Perform TDR test for all signal layers.
    Present TDR test results for all signal layers.

BOARD's DRILL SCHEDULE: Layer_1 to Layer_8

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
⊞	.0094	1150	YES	---	

BOARD's DRILL SCHEDULE: Layer_9 to Layer_16

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.0092	1195	YES	---	

BOARD's DRILL SCHEDULE THRUHOLE: Layer_1 to Layer_16

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
⌀	.0132	922	YES	---	
⊟	.035	132	YES	---	
⊖	.041	50	YES	---	
◫	.057	6	YES	---	
⊕	.098425197	2	YES	---	
□	.15	2	NO	---	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	9/27/2011
CHECKED M.Bogdan	9/27/2011
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DRS4-16Ch Module
Specification Drawing

SIZE | FSCM NO. | DWG. NO. 2749 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED