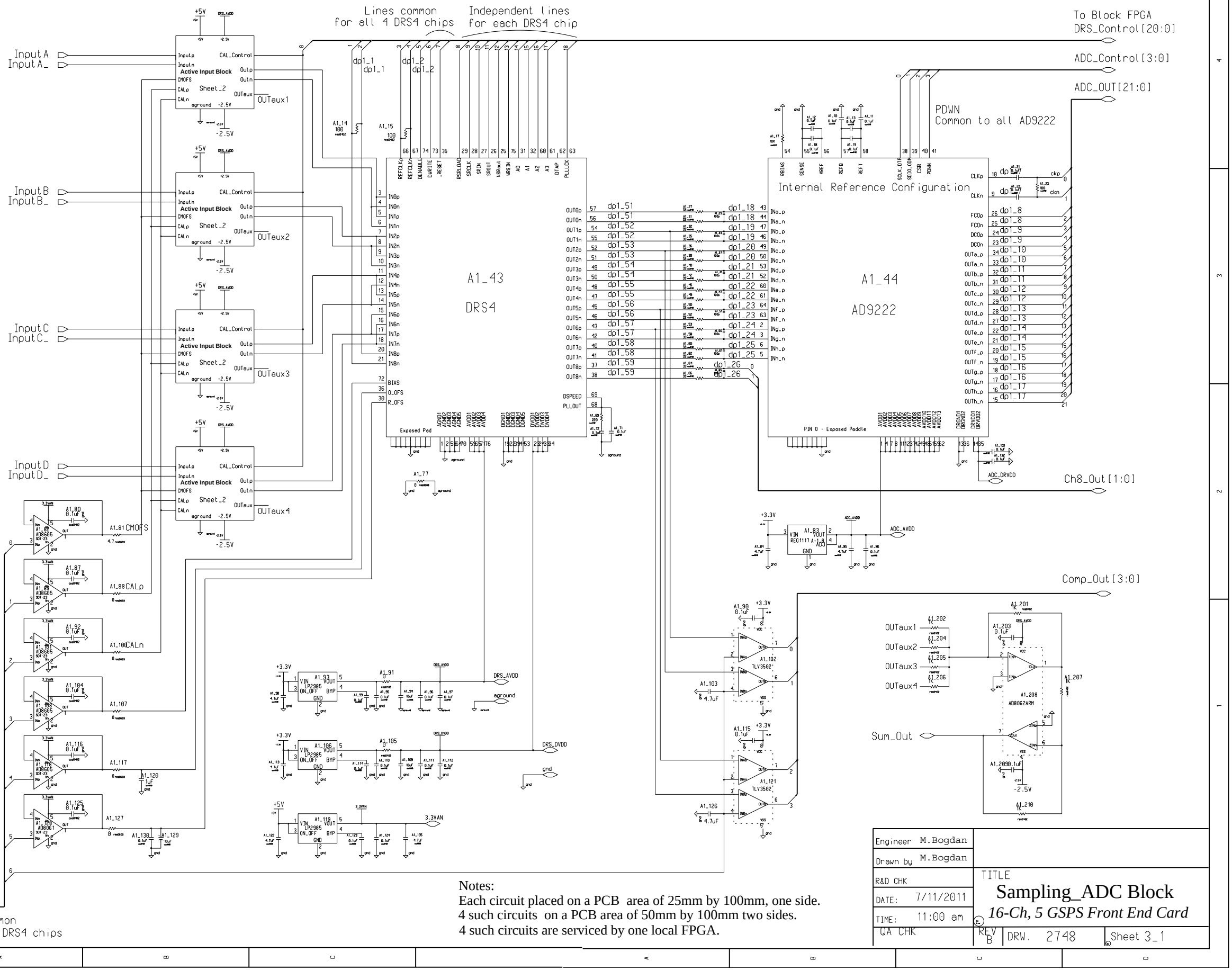
Lines common
for all 4 DRS4 chips
Independent lines
for each DRS4 chip
To Block FPGA
DRS_Control[20:0]
ADC_Control[3:0]
ADC_OUT[21:0]
PDWN
Common to all AD9222
InputA
InputA_
InputB
InputB_
InputC
InputC_
InputD
InputD_
Active Input Block
Sheet_2
OUTaux1
OUTaux2
OUTaux3
OUTaux4
CMOFS
CALp
CALn
-2.5V
A1_43
DRS4
A1_44
AD9222
Internal Reference Configuration
Exposed Pad
PIN 0 - Exposed Paddle
ADC_DRVDD
ADC_AVDD
Ch8_Out[1:0]
Comp_Out[3:0]
Sum_Out
DRS_AVDD
DRS_DVDD
3.3VAN
DAC[7:0]
Lines common
for all 4 DRS4 chips
Notes:
Each circuit placed on a PCB area of 25mm by 100mm, one side.
4 such circuits on a PCB area of 50mm by 100mm two sides.
4 such circuits are serviced by one local FPGA.
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 7/11/2011
TIME: 11:00 am
QA CHK
TITLE
Sampling_ADC Block
16-Ch, 5 GSPS Front End Card
REV B
DRW. 2748
Sheet 3_1