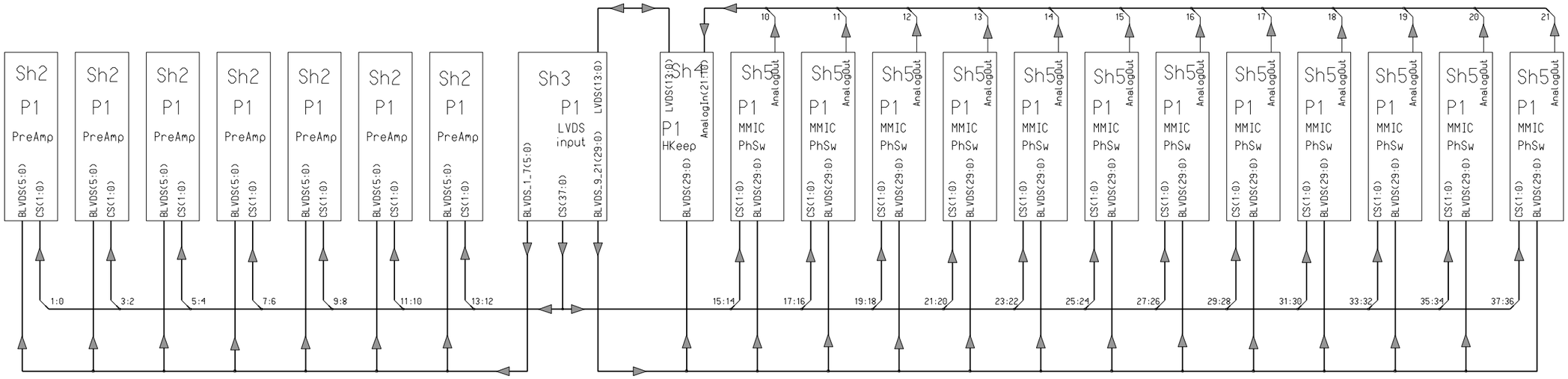
Slot1 Slot2 Slot3 Slot4 Slot5 Slot6 Slot7 Slot8 Slot9 Slot10 Slot11 Slot12 Slot13 Slot14 Slot15 Slot16 Slot17 Slot18 Slot19 Slot20 Slot21

LVDS(13:0)

I/O LVDS lines
-6 inputs: A8,...,A11,DCLK,CNV.
-1 output: LVDS_OUT

AnalogInput(21:10)

One Analog Signal from each Module in Slot 10,...,21 to the HKeep Card.
All signals are referenced to the common AGND plane.



BLVDS_1_7(5:0)

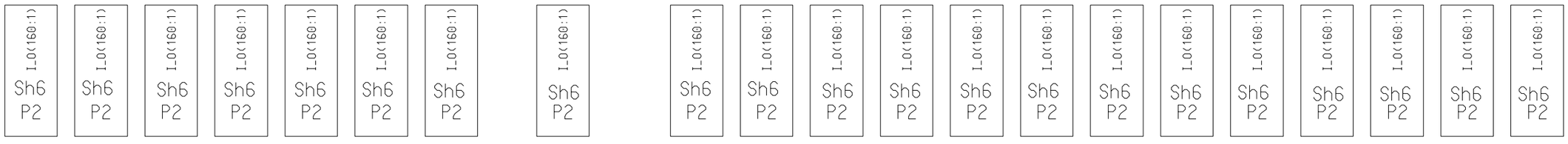
-3 BLVDS inputs: SCK,CLR,DIN.
Note: These inputs are the same as in BLVDS_9_21.
They are doubled in the LVDS input SAB.

CS(37:0)

-19 LVDS inputs.
-one for each PreAmp, MMIC and PhSw card.

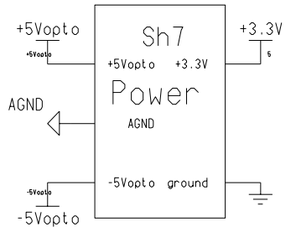
BLVDS_9_21(29:0)

-15 BLVDS inputs: SCK,CLR,DIN,A0,...,A7,PCLK0A,PCLK1A,PCLK0B,PCLK1B.



Notes:

2. All P2 pins feed through and do not connect to the Backplane.
3. "+3.3V" and "ground" are digital power and ground planes, common for all modules.
4. "+5Vopto", "-5Vopto" and "GNDopto" are local power and ground planes common for MMIC, PhSw and HKeeper Modules.
5. All BLVDS signals are driven each by an DS92001 Buffer, located on the Slot 8 SAB and are termineted on the Backplane. They shall not be terminated on Modules. BLVDS inputs: SCK,CLR,DIN are doubled inside the Slot 8 SAB.
6. All LVDS inputs are poin-to-point and have to be terminated on Modules.



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Drawn by M.Bogdan		
R&D CHK	TITLE	Size C
DATE: 5/10/05	Top Level *QEB-Backplane*	
TIME: 2:00 pm		
QA CHK	REV A / DRW. B-2563	Sheet 1 of 7