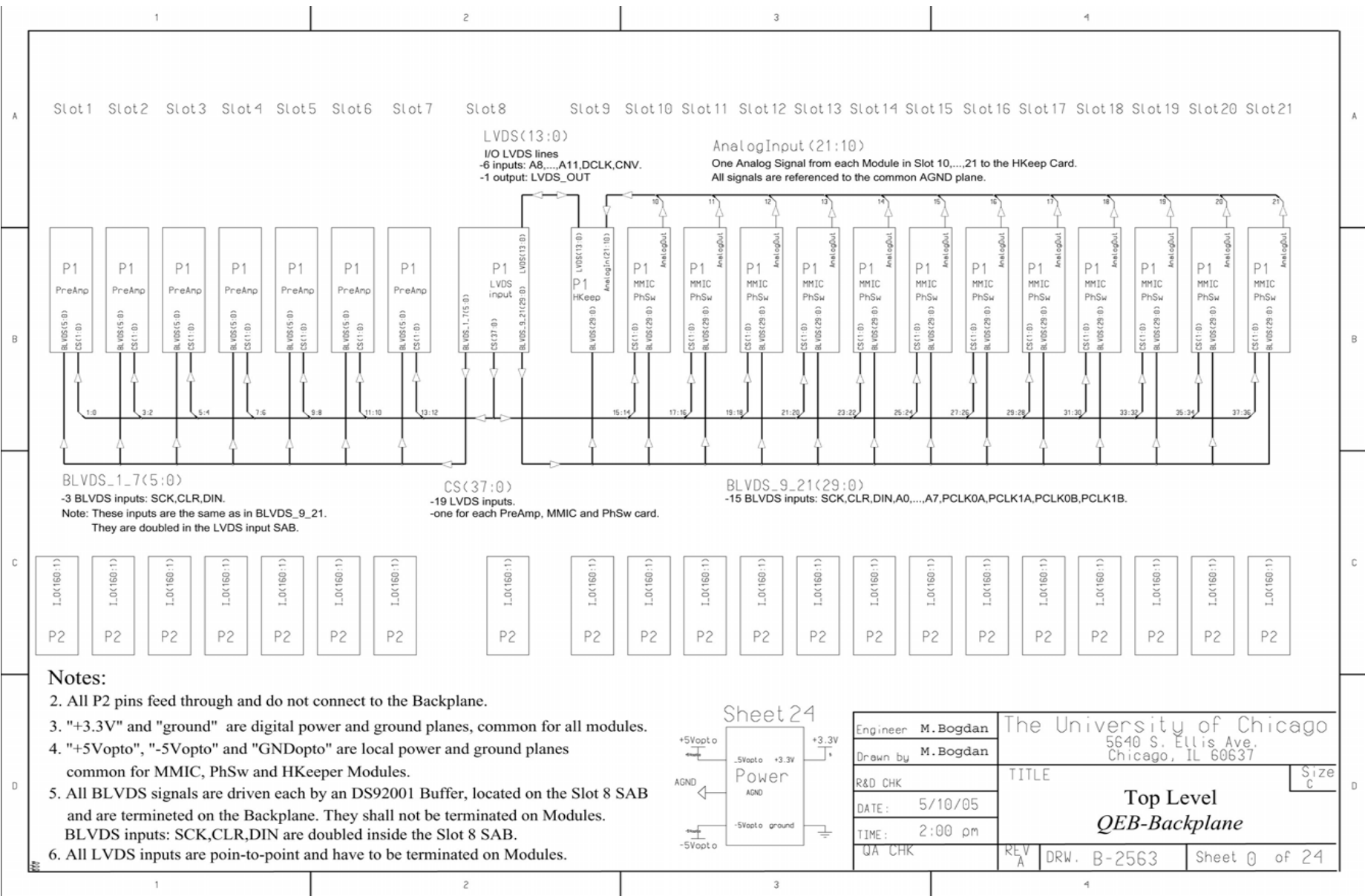


# The QUIET Electronics Box Implementation - I



Slot1 Slot2 Slot3 Slot4 Slot5 Slot6 Slot7 Slot8 Slot9 Slot10 Slot11 Slot12 Slot13 Slot14 Slot15 Slot16 Slot17 Slot18 Slot19 Slot20 Slot21

LVDS(13:0)  
I/O LVDS lines  
-6 inputs: A8,...,A11,DCLK,CNV.  
-1 output: LVDS\_OUT

AnalogInput(21:10)  
One Analog Signal from each Module in Slot 10,...,21 to the HKeep Card.  
All signals are referenced to the common AGND plane.

BLVDS\_1\_7(5:0)

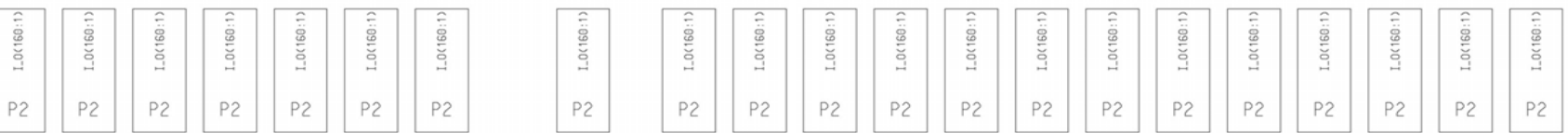
-3 BLVDS inputs: SCK,CLR,DIN.  
Note: These inputs are the same as in BLVDS\_9\_21.  
They are doubled in the LVDS input SAB.

CS(37:0)

-19 LVDS inputs.  
-one for each PreAmp, MMIC and PhSw.

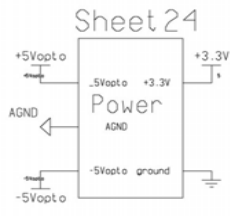
BLVDS\_9\_21(29:0)

-15 BLVDS inputs: SCK,CLR,DIN,A0,...,A7,PCLK0A,PCLK1A,PCLK0B,PCLK1B.



**Notes:**

- All P2 pins feed through and do not connect to the Backplane.
- "+3.3V" and "ground" are digital power and ground planes, common for all modules.
- "+5Vopto", "-5Vopto" and "GNDopto" are local power and ground planes common for MMIC, PhSw and HKeeper Modules.
- All BLVDS signals are driven each by an DS92001 Buffer, located on the Slot 8 SAB and are terminated on the Backplane. They shall not be terminated on Modules. BLVDS inputs: SCK,CLR,DIN are doubled inside the Slot 8 SAB.
- All LVDS inputs are point-to-point and have to be terminated on Modules.



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Drawn by	M. Bogdan			
R&D CHK		TITLE	Size C	
DATE:	5/10/05	<b>Top Level</b> <i>QEB-Backplane</i>		
TIME:	2:00 pm			
QA CHK		REV A	DRW. B-2563	Sheet 0 of 24

# QEB – Power/pins requirements

MMIC Bias Interface Boards(7 boards):

-total power: 350mW x 14 modules x 7 PCBs = 34.3W

-current from isolated power supplies:

14 floating power supplies @ 3.5V/600mA - 28 pins/600mA each;

14 floating power supplies @ 5V/25mA - 28 pins/25mA each.

PhSw Interface Boards(5 boards):

-total power: ~2.5W/PCB x 5 PCBs = 12.5W

-current from isolated power supplies:

30 floating power supplies @ 5V/50mA - 60 pins/50mA each

PreAmp Boards (7 boards each):

- total power: 7W/PCB x 7PCBs = 50W

-current from isolated power supplies:

28 floating power supplies @ 5V/0.5A - 56 pins/1A each

HouseKeeping board:

- total power not specified; guess: 5W – no extra pins

Shared digital: 3.3V/3A: 10W - 8 pins/1A each

Shared analog: ±5V/1A: 10W - 8 pins/1A each.

~120W

## Total Pins

•72 pins – 1A

•28 pins – 600mA

•28 pins – 25mA

•60 pins – 50 mA

•90 pins LVDS data

-----  
278 pins total

# Cables & Connectors

- Analog data: 12 pc. Pave Tech. Micro D 100 pins
  - quote for hermetic connector and wires inside dewar (twisted pairs, individually shielded, shield goes to pin)
  - no quote for the exterior cables yet (100 pin Micro D to 78 pin)
- Power: 3 pc. Glenair Bulkhead Feed-Thru Hermetic 947-115 series, 79 pins
  - quote for hermetic connectors with cables to inside/outside, no end of cables (cryostat design change required!)
- LVDS: 1 pc. Pave Tech Micro D, twin-connector 2x51 pins
  - quote in progress for twisted pairs

## Yet to be defined:

- shielding of power cables (Twisted pairs with shields? Faraday-cage? Braid?)
- cables for power and LVDS outside dewar ('hydra-cables' required going e. g. from 2 to 3 connectors or some kind of 'breakout box')

# Power Supplies

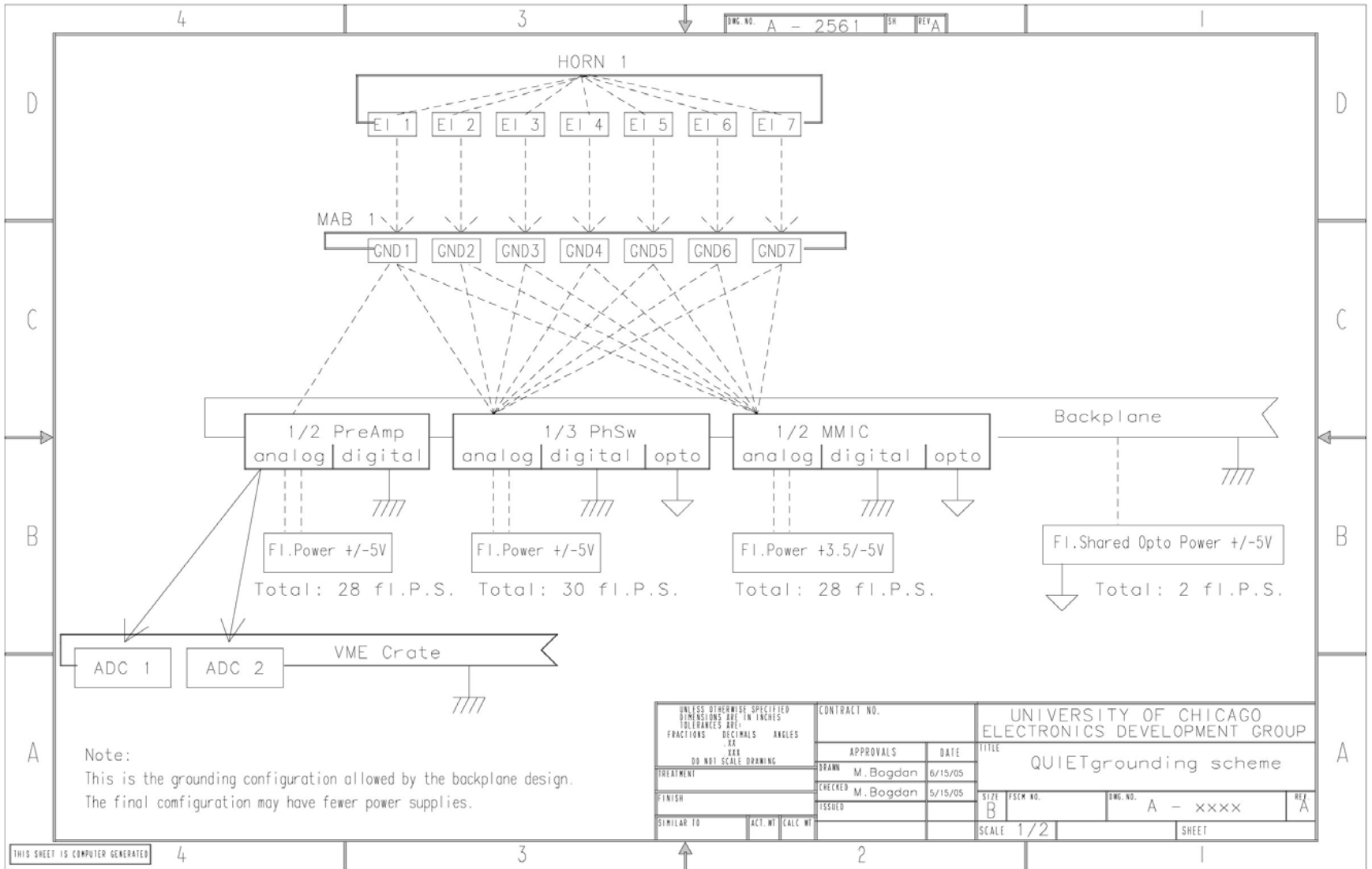
## Outside power supplies needed:

- 14 floating power supplies: 3.5V/1A each (for MMIC);
- 28 floating power supplies: 5V/1A each (for PreAmps);
- 44 floating power supplies: 5V/50mA each (for MMIC and PhSw);
- 2 floating power supplies: 5V/3A each (for shared analog);
- one regular power supply: +3.3V/3A (for shared logic).

Ex.: Acopian 5EB100: 5V/1A, Linear Regulated, ripple: 1mV RMS, temp coefficient: 0.03%/degC.

size: 1.6" x 2.5" x 3.5" => 24 pieces on a 16" by 15" plate, can stack up the plates.

**Worst case scenario:** All power supplies occupy a volume the size of a 6U VME Crate.



Note:  
 This is the grounding configuration allowed by the backplane design.  
 The final configuration may have fewer power supplies.

<small>UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX .XX .XX DO NOT SCALE DRAWING</small>	CONTRACT NO.		UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP	
	APPROVALS		DATE	TITLE
	DRAWN M. Bogdan		6/15/05	QUIETgrounding scheme
	CHECKED M. Bogdan		5/15/05	
FINISH	ISSUED	SIZE B	FSCM NO.	DWG. NO. A - xxxx
SIMILAR TO	ACT. WT	CALC. WT	SCALE 1/2	SHEET