Schematic Drawing: B - 2572
Assembly Drawing: A - 2574

1.650

4.000

AUX Card Drill Schedule (inches)

<table>
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<tr>
<th>FMS</th>
<th>COUNT</th>
<th>PLATED</th>
<th>DRILL SYMBOL</th>
<th>COMMENT</th>
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Layer Order:
1. Signal 1
2. Power: 4.3V
3. Signal 2

Board Characteristics:
2. Board Thickness: 0.062"/0.005" (1.57 +/- 0.13mm).
3. Minimum Trace Width/Clearance: 0.006".
4. 1 oz Copper for top, bottom and power layers.
5. 1/2 oz Copper for embedded signal layers.
6. Solder plating; apply solder mask.
7. Silk screen on both sides.
8. Interlayer spacing: as specified.
9. FMS tolerances: +/- 0.005" unless specified otherwise.
10. Trace impedance: Zc = 55 Ohms +/- 10%.
11. Perform TDR tests and present test results.

THE UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

OERS - LVDS 1/0 - SAB
Specification Drawing