CDF Drift Chamber Signal Analyzer Board

Bill Ashmanskas
Mircea Bogdan
Henry Frisch
Aseet Mukherjee
Harold Sanders
Mel Shochet
CDF Drift Chamber Signal Analyzer Board
Drift Chamber Signals – Fe55 pulses

Six-channel scope:

- Designed for CDF Central Calorimeter and COT crates;
- Use of limited +5V power;
- 4-buffer CDF/VME readout;
- Bandwidth: 100MHz @ 3dB;
- Input: [-150;+50]mV;
- 8-Bit, 500MHz FADC;
- Triggered by L1,L2 Accept;
- Samples delayed/buffered in a ~5.5 us pipeline;
- 132 ns CDF clock markers.
CDF Drift Chamber Signal Analyzer Board
Block Diagram

- 6 A/D Channels;
- 6 Data Buffers;
- 495.8 MHz ECL Crystal Oscillator;
- Power Block: +3.3V & +2.5V;
- VME Interface with Altera-EPM7128S.
CDF Drift Chamber Signal Analyzer Board
Analog/Digital Conversion Channel

- Gain = 10;
- Offset = -0.5V;
- 500MHz FADC;
- 2x8-Bit ECL Buses at 250MHz;
- 2x16-Bit TTL Buses at 125MHz;
- 5V/5.2V - 3A DC/DC converters;
- +/- 4.6V linear power with LDO.
CDF Drift Chamber Signal Analyzer Board
Data Buffer Channel

- Input: four 8-bit data banks, 2 ns apart, at 125 MHz;
- ACEX1K30TC144-1 - splits data into a 64-bit bus at 62.5MHz
- APEX 20K200BC356-1 - delays and buffers data for VME readout.

June 4-8, 2001
Valencia, Spain

Mircea Bogdan, RT2001
CDF Drift Chamber Signal Analyzer Board
Test pulse

Overlay:
- Test pulse generated with LeCroy9211 and sampled with a two-channel prototype board.