CDF Drift Chamber Signal Analyzer Board

Bill Ashmanskas, Mircea Bogdan, Henry Frisch, Aseet Mukherjee, Harold Sanders, Mel Shochet

Abstract--**The Collider Detector at Fermilab is a 5000-ton magnetic spectrometer designed to study 2 TeV proton-antiproton collisions at luminosities exceeding $10^{32}/cm^2/sec$. Deriving measurements of physical phenomena from CDF data requires a detailed understanding of the spectrometer's response to charged particles. Using commercially available flash ADCs and FPGAs, we have designed and built a VME module to record and buffer 8-bit samples of six analog drift chamber signals at 500 MSPS. Full integration with CDF's pipelined data acquisition system allows oscilloscope-quality data to be correlated with particle trajectories reconstructed in the Central Outer Tracker. These data will be a valuable tool for tuning particle-level simulations of the COT. The paper describes the design of the COT Signal Analyzer board and presents prototype results.**

I. INTRODUCTION

The Central Outer Tracker of the newly upgraded CDF detector measures charged particle trajectories with ~200μm precision at 96 measurement layers, between 40cm and 135cm from the nominal beamline. All 30240 COT channels are instrumented with amplifier-shaper-discriminator circuitry and time-to-digital converters with 1ns granularity. 96 channels are also instrumented for analog pulse readout through amplifiers and analog multiplexers. Of these 96 analog outputs, 26 will be digitized by Signal Analyzer (FADC) boards. Using the 8-bit, 500 MSPS FADC data, one can study the ASD/TDC response in detail on a small number of channels, and then apply the resulting knowledge to the full set of 30240 channels.

The COT will play a key role in forthcoming high-statistics measurements of heavy quark and weak boson properties and in searches for phenomena beyond the standard model of particle interactions. A well-tuned model of COT track measurement may reduce the effort needed to turn data from the upgraded CDF detector into publishable results. We list several examples below.

Many measurements use specific ionization (dE/dx) in the drift chamber to distinguish particle species. Calibrating dE/dx response requires an understanding of many contributions to pulse shape: track incidence angle, electronics response, fluctuations in the deposition and drift of ionization, and of course specific ionization. A detailed model of these effects has been developed by the COT's designers. FADC data will allow this model to be tested with real pulses from particles of known species (e.g. from resonance decay), as part of the dE/dx calibration process.

In addition, many decay modes of the top quark or the (yet undiscovered) Higgs boson produce high-momentum bottom quarks, whose decay products must be reconstructed within dense jets of particles. Predicting the efficiency of this reconstruction requires a reliable model for the drift chamber's ability to distinguish the pulses produced by two nearby charged particles. By correlating oscilloscope-quality digitized pulses with tracks reconstructed in collision data, one can characterize in detail the two-track separation ability of the COT.

Finally, secondary particles produced in the inner detector material can affect the reconstruction even of relatively isolated particles, such as electrons and muons from W boson decay. Examining pulse data for isolated, high-momentum tracks will provide a useful check of detector-material effects in the simulation.

II. BLOCK DIAGRAM

The Block Diagram of the Signal Analyzer Board is presented in Fig. 1. The 500 MHz crystal-controlled ECL-compatible oscillator provides the clock for the six identical channels, via a differential clock driver. Each channel includes a full parallel (flash) analog-to-digital converter capable of digitizing full-scale (-0.150V to +0.050V at the board input) inputs into eight-bit digital words with a 2 nsec sampling period. After conversion, the data are successively demultiplexed, converted to TTL, delayed, buffered, and made ready for readout via the VME interface.

To synchronize with CDF's deadtimeless trigger and DAQ system, samples must be acquired continuously and delayed in a ~5.5μsec pipeline, awaiting the Level 1 trigger decision, which is issued at 132 nsec intervals, with ~42 period latency. Upon Level 1 accept, data from the end of the pipeline are routed to one of four VME-accessible DAQ buffers (selected by the trigger system); upon Level 1 reject, data simply spill off the end of the pipeline. If Level 2 accepts an event, the corresponding buffer is read via VME; if Level 2 rejects the event, the buffer is simply reused. The Signal Analyzer's DAQ buffers are deep enough to hold 1024 samples (2048 nsec), allowing one to study the effect of previous beam crossings on the current event.

Bill Ashmanskas, Mircea Bogdan, Henry Frisch, Harold Sanders, Mel Shochet are with The University of Chicago, 5640 S. Ellis Ave., Chicago, IL 60637; Aseet Mukherjee is with Fermi National Accelerator Laboratory, Batavia, IL 60510.
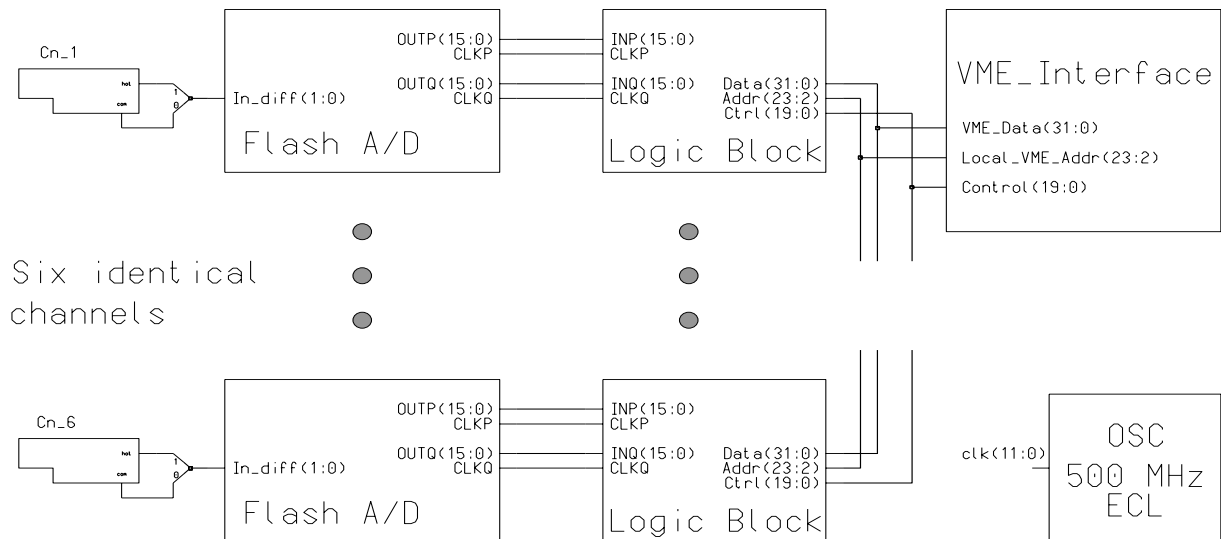
Fig.1 Block Diagram

Because the four memory buffers function independently, the board places no restrictions on the relative times of Level 1 accepts to different memory buffers. Because the on-board oscillator is not synchronized to the 132 nsec CDF clock, a time marker signal, derived from the 132 nsec clock, is injected in parallel with the FADC input.

III. IMPLEMENTATION

Fig. 2 presents the schematic of one analog–to-digital converter channel. The eight-bit 500 MSPS Flash A/D Converter U3 [1] receives the analog signal through a low-distortion differential line receiver U4 [2] followed by the op amp U5 in a typical non-inverting configuration [3] that provides clamping and also has a –0.5V offset. This input
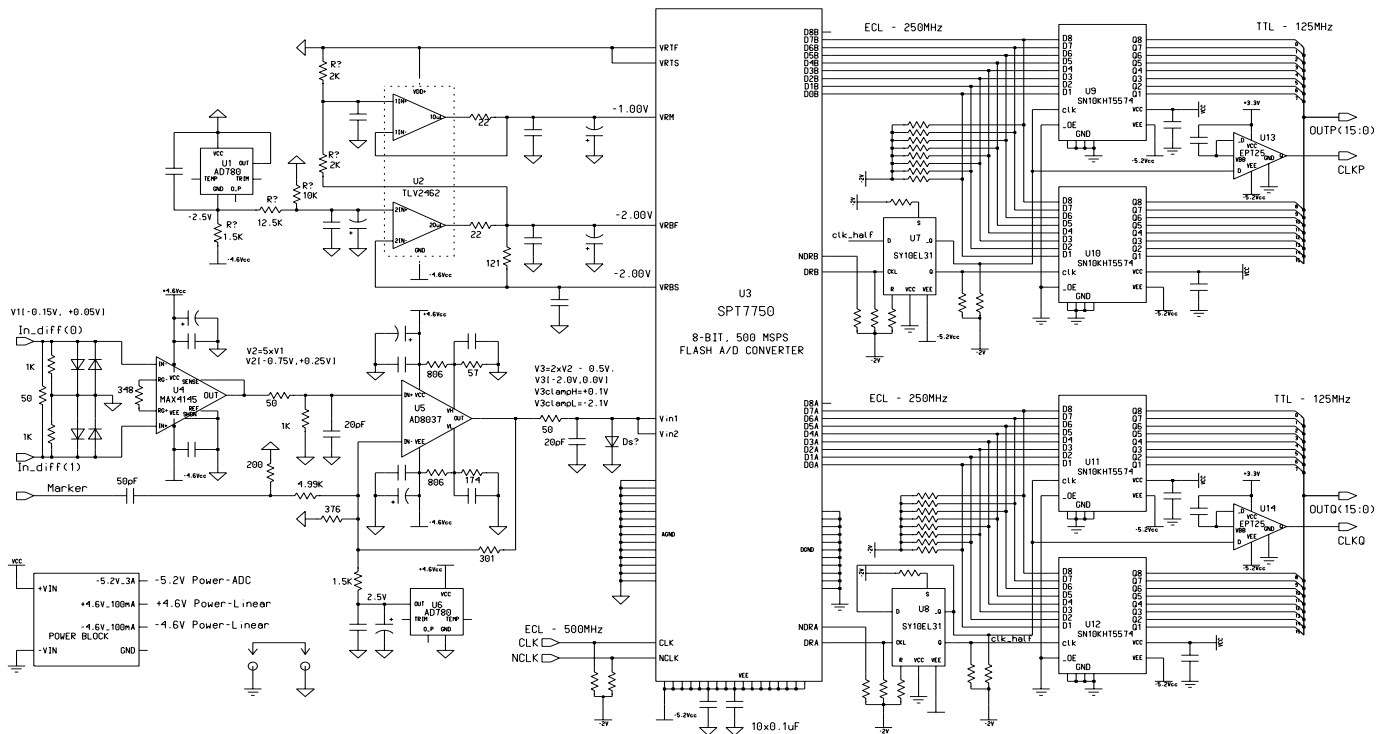

Fig.2 Analog Channel

amplifier circuit provides a gain of 10 and a bandwidth of 100 MHz at –3 dB.

U1 and U2 provide the –1V and –2V voltages applied across the internal reference ladder of the Flash A/D

converter U3. The ECL-compatible digital outputs are split into two banks of eight-bit, gray code formatted words. Each bank is updated at ½ the input clock rate and has inverted phase.

With U9,…,U12, the digital signals are converted to TTL and demultiplexed again into four buses, reducing the frequency to 125 MHz.

In order to accommodate the existing power resources of the Central Calorimeter Crate and of the COT TDC Crate at CDF, each channel is provided with its own DC/DC converter that generates the –5.2V for the ECL logic. To minimize the noise level, the input amplifier is powered locally with linear circuits.

Each logic block contains two Altera FPGAs. An ACEX 1K30TC144-1 [4] chip receives, in parallel, four eight-bit samples, 2nsec apart in phase, updated at 125 MHz, and demultiplexes them into 64 data bits, updated at 62.5 MHz. On this eight-sample bus, the four odd FADC samples are 2nsec behind the four even FADC samples, because of the separate data paths and clock signals used for odd and even samples.

A second Altera chip, APEX 20K200BC356-1XV [5], receives, delays, and records sets of eight samples at 62.5 MHz. An internal dual-ported memory, 64 bits wide and 512 words deep, implements the ~5.5μsec delay as a circular memory buffer, with a constant offset between read and write addresses. Four additional dual-ported memories, 64 bits wide and 128 words deep, implement the DAQ buffers, with write addresses generated by counting clock cycles since the corresponding Level 1 accept signals and read addresses derived from the VME address bus.

We have implemented the most speed-critical data capture functionality within a small, fast chip, whose firmware is unlikely to evolve. This choice afforded us much more freedom in selecting a large chip for data buffering, and reduces our concern about the effects of future firmware changes on timing within the large chip.

As of the time of this writing, we have built and tested a two-channel prototype board and are producing four six-channel boards. Fig. 3 shows a pulse sampled with the two-channel prototype. The r.m.s. noise level on the prototype is 1.5 ADC counts, dominated by 125 MHz digital noise. We have optimized filters and reduced input trace lengths for the production design, and hope to achieve a noise level below one ADC count.
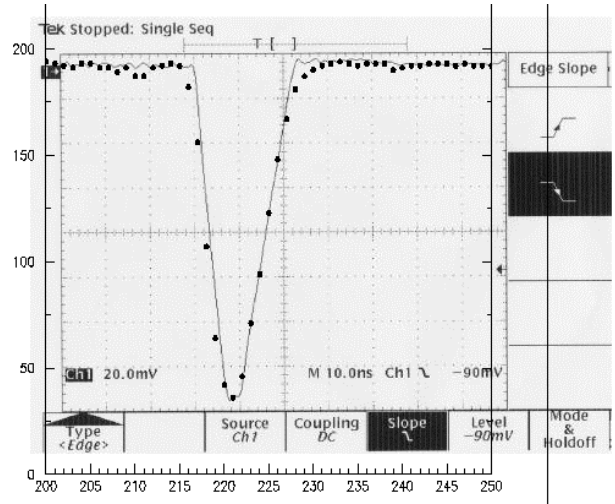

Fig. 3 Test pulse sampled with the two-channel prototype.

IV. CONCLUSION

We have designed and tested a board, using the 8-bit, 500 MSPS SPT 7750 Flash ADC chip for sampling and Altera 1K30 and 20K200 FPGAs for data processing, to record oscilloscope-quality drift chamber pulse data into the event data stream of the CDF detector. Correlating FADC pulse data with reconstructed tracks will provide valuable checks of the simulation and calibration of CDF's Central Outer Tracker.

V. REFERENCES

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