



Processor Block

Sheet 19,20,21,22,23

VME_Data[31:0]
 VME_Addr[26:2]
 VME_AUX[10:0]
 Clocks1[8:0]
 Clocks2[8:0]
 Clocks3[8:0]
 Clocks4[8:0]
 HOLDtoAMB[15:0]
 FREEZEin
 FREEZEout
 RxAMB[31:0]
 RxHS[23:0]
 InternalAUXbus[7:0]
 Gendatain[7:0]

Input Block

Sheet 12,13,14,15,16

InternalAUXbus[7:0]
 Gendataout[7:0]
 HOLDfromProcessors[47:0]
 TxHS[23:0]
 Clocks5[7:0]
 Clocks6[7:0]
 VME_Data[31:0]
 VME_Addr[26:2]
 VME_AUX[10:0]
 SFP_Rx[1:0]
 SFP_Tx[1:0]
 SFP_Control[7:0]
 FREEZEin
 FREEZEout
 HOLDfromAMB[11:0]
 QSFPRx0[7:0]
 QSFPTx0[7:0]
 QSFPControl0[6:0]
 TxAMB[23:0]
 QSFPRx1[7:0]
 QSFPTx1[7:0]
 QSFPControl1[6:0]

VME Interface

Sheet 2,3

VME_Data[31:0]
 VME_Addr[26:2]
 VME_AUX[10:0]
 P2[159:0]
 VME_P2(159:0)
 HOLDtoAMB[15:0]
 FREEZEtoRxTx
 FREEZEfromRx
 FREEZEfromTx
 HOLDfromAMB[11:0]

Clk

Sheet 24

Out1[8:0]
 Out2[8:0]
 Out3[8:0]
 Out4[8:0]
 Out5[7:0]
 Out6[7:0]

RxBuffer

Sheet 5

IN[31:0]
 OUT[31:0]

TxBuffer

Sheet 6

IN[23:0]
 OUT[23:0]

RP3

Sheet 4

From_AMBoard[31:0]
 To_AMBoard[23:0]

RP0

Sheet 7

VME_P8(94:0)

Power

Sheet 8,9,10,11

+5V
 GND

Top_Tracks[7:0]
 Top_HOLDfromSFP
 Top_HOLDtoHS[47:0]
 Top_Gendata[7:0]
 HS
 TTL
 HS

SFP

Sheet 17

Rx[1:0]
 Tx[1:0]
 Control[7:0]

QSFP

Sheet 18_1

Rx[7:0]
 Tx[7:0]
 Control[6:0]

QSFP

Sheet 18_2

Rx[7:0]
 Tx[7:0]
 Control[6:0]

Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE	Top Level
DATE:	1/25/13	FTK-AM-AUX Card	
TIME:	9:25 am	REV	A
		DRW.	2808 Sheet 1/24