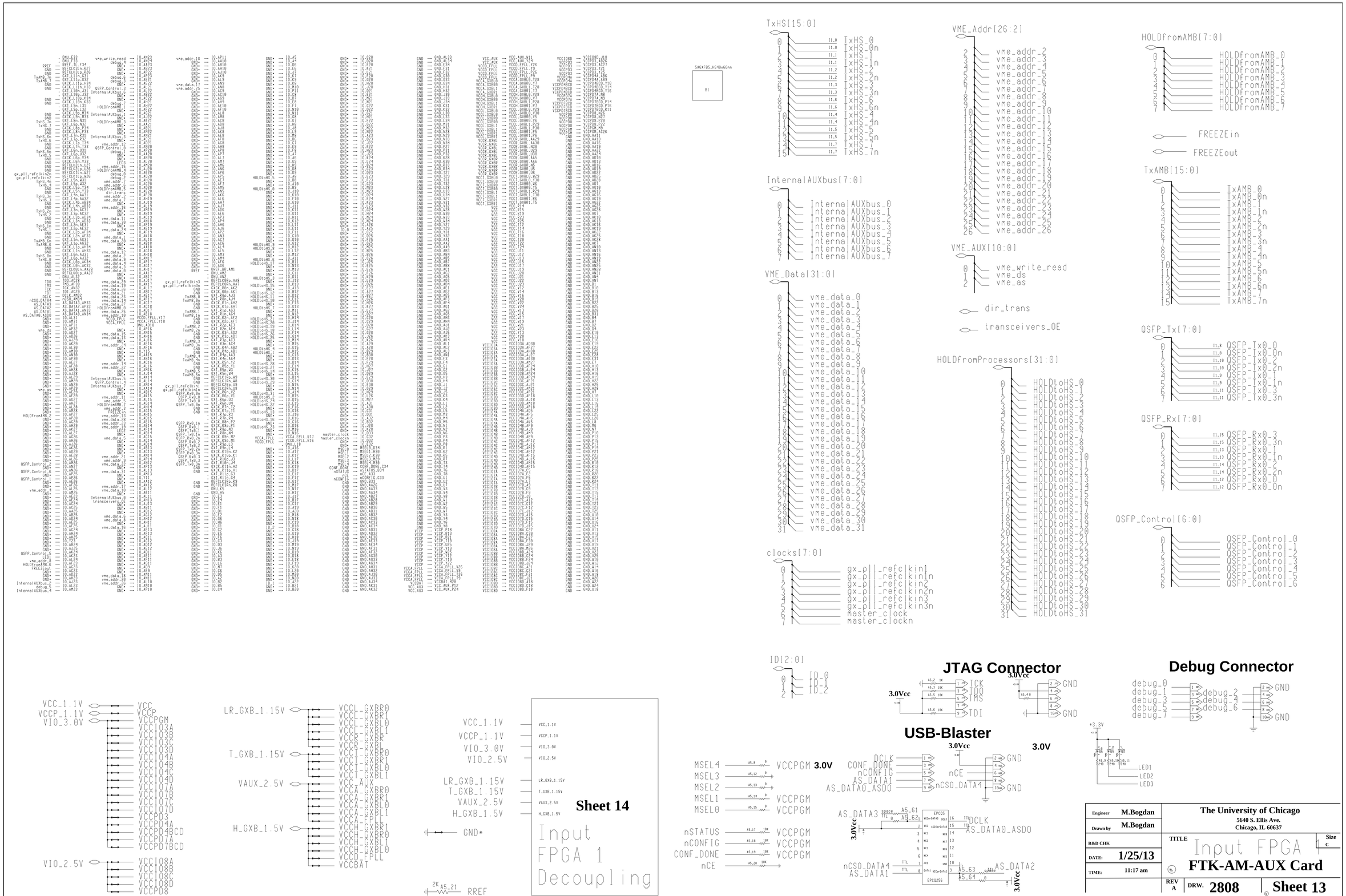
TxHS[15:0]
VME_Addr[26:2]
HOLDfromAMB[7:0]
FREEZEin
FREEZEout
TxAMB[15:0]
InternalAUXbus[7:0]
VME_Data[31:0]
VME_AUX[10:0]
dir_trans
transceivers_OE
QSFP_Tx[7:0]
HOLDfromProcessors[31:0]
QSFP_Rx[7:0]
QSFP_Control[6:0]
clocks[7:0]
ID[2:0]
JTAG Connector
Debug Connector
USB-Blaster
3.0Vcc
3.0V
VCC_1.1V
VCCP_1.1V
VIO_3.0V
VIO_2.5V
LR_GXB_1.15V
T_GXB_1.15V
VAUX_2.5V
H_GXB_1.5V
GND*
RREF
Sheet 14
Input FPGA 1 Decoupling
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 1/25/13
TIME: 11:17 am
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE Input FPGA 1
FTK-AM-AUX Card
Size c
REV A
DRW. 2808
Sheet 13