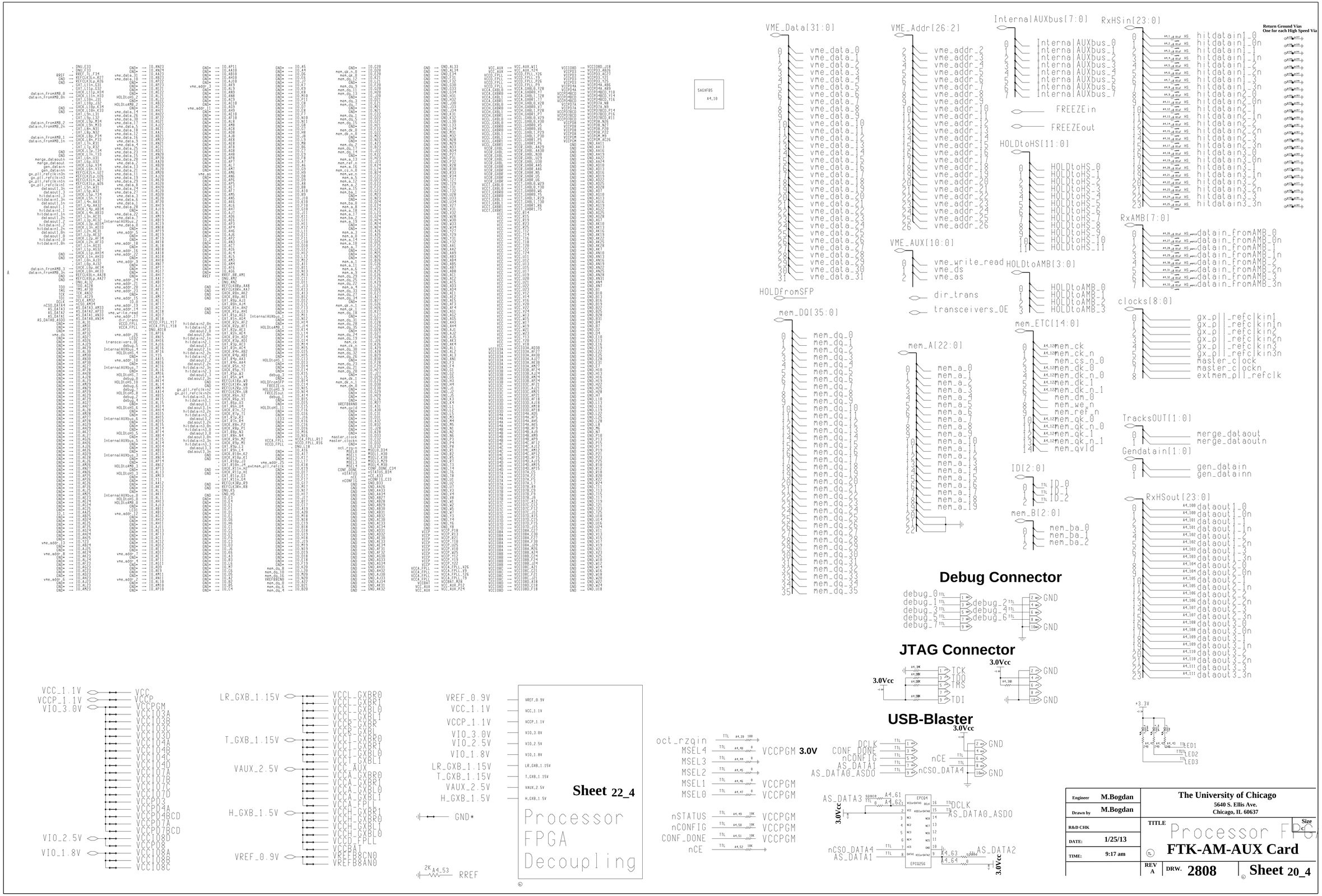

VME_Data[31:0]
VME_Addr[26:2]
InternalAUXbus[7:0]
RxHSin[23:0]
Return Ground Vias
One for each High Speed Via
FREEZEin
FREEZEout
HOLDtoHS[11:0]
RxAMB[7:0]
VME_AUX[10:0]
HOLDtoAMB[3:0]
clocks[8:0]
HOLDfromSFP
mem_DQ[35:0]
mem_A[22:0]
mem_ETC[14:0]
TracksOUT[1:0]
Gendatain[1:0]
ID[2:0]
mem_B[2:0]
RxHSout[23:0]
Debug Connector
JTAG Connector
USB-Blaster
3.0Vcc
3.0V
Sheet 22_4
Processor
FPGA
Decoupling
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 1/25/13
TIME: 9:17 am
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Processor FPGA
FTK-AM-AUX Card
REV A
DRW. 2808
Sheet 20_4