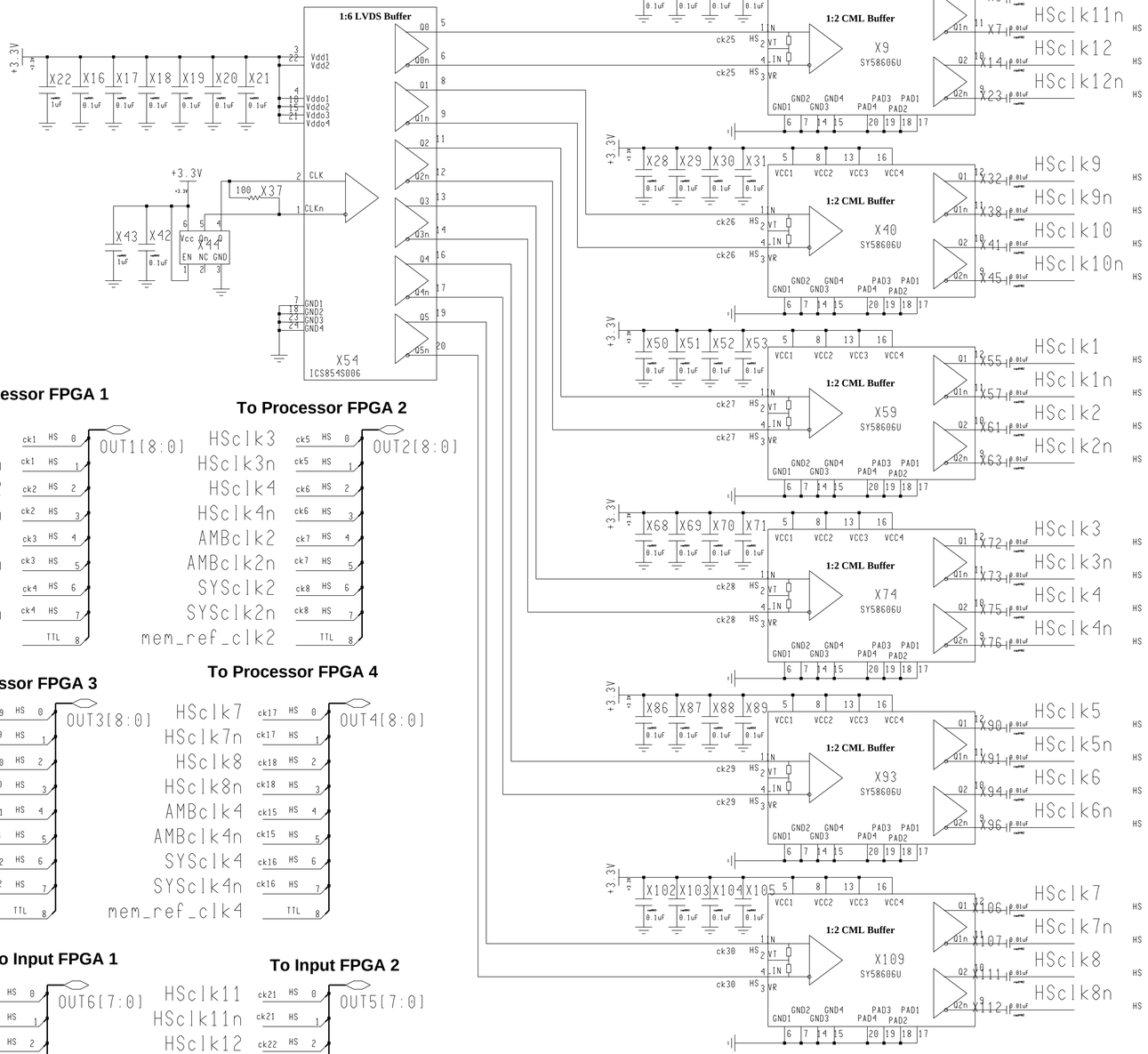
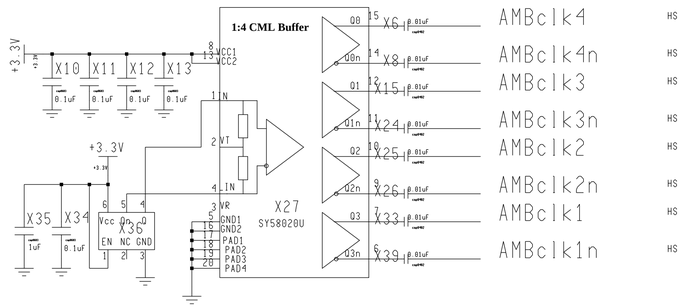
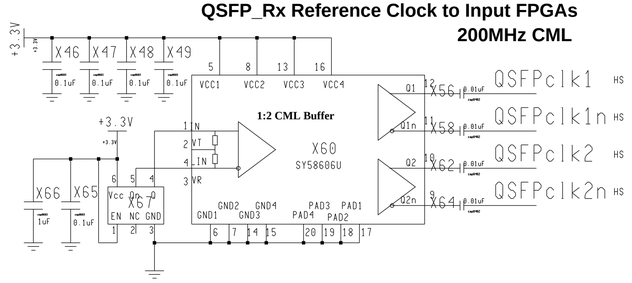
HS Reference Clock to all FPGAs
200MHz CML



AMB Reference Clock to Processor FPGAs
100MHz CML



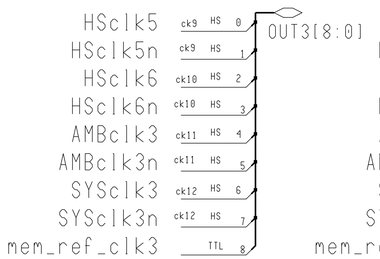
QSFP_Rx Reference Clock to Input FPGAs
200MHz CML



To Processor FPGA 1

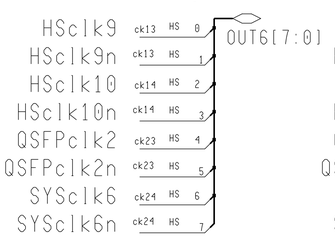
To Processor FPGA 2

To Processor FPGA 3

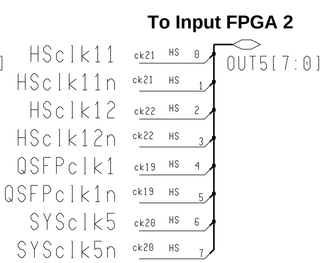


To Processor FPGA 4

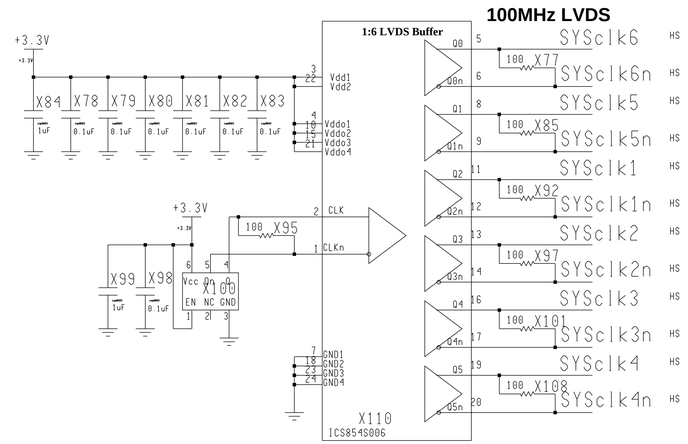
To Input FPGA 1

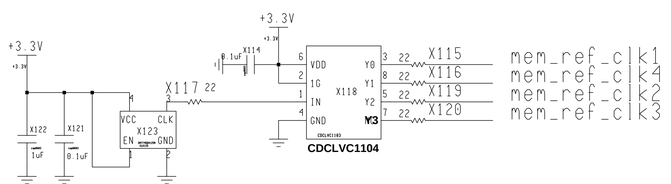


To Input FPGA 2



Internal Clock to all FPGAs
100MHz LVDS





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Drawn by	M.Bogdan		
R&D CHK		TITLE Clocks FTK-AM-AUX Card	Size C
DATE:	1/25/13		
TIME:	10:17 am		
		REV A / DRW. 2808	Sheet 24