



IN[23:0]

OUT[23:0]

Tx: to Front Module

Tx: From Local FPGA

Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637			
Drawn by	M.Bogdan				
R&D CHK		TITLE	Size C		
DATE:	1/15/13	Tx Buffers FTK-AM-AUX Card			
TIME:	1:48 pm				
REV	A	DRW.	2808	Sheet	6