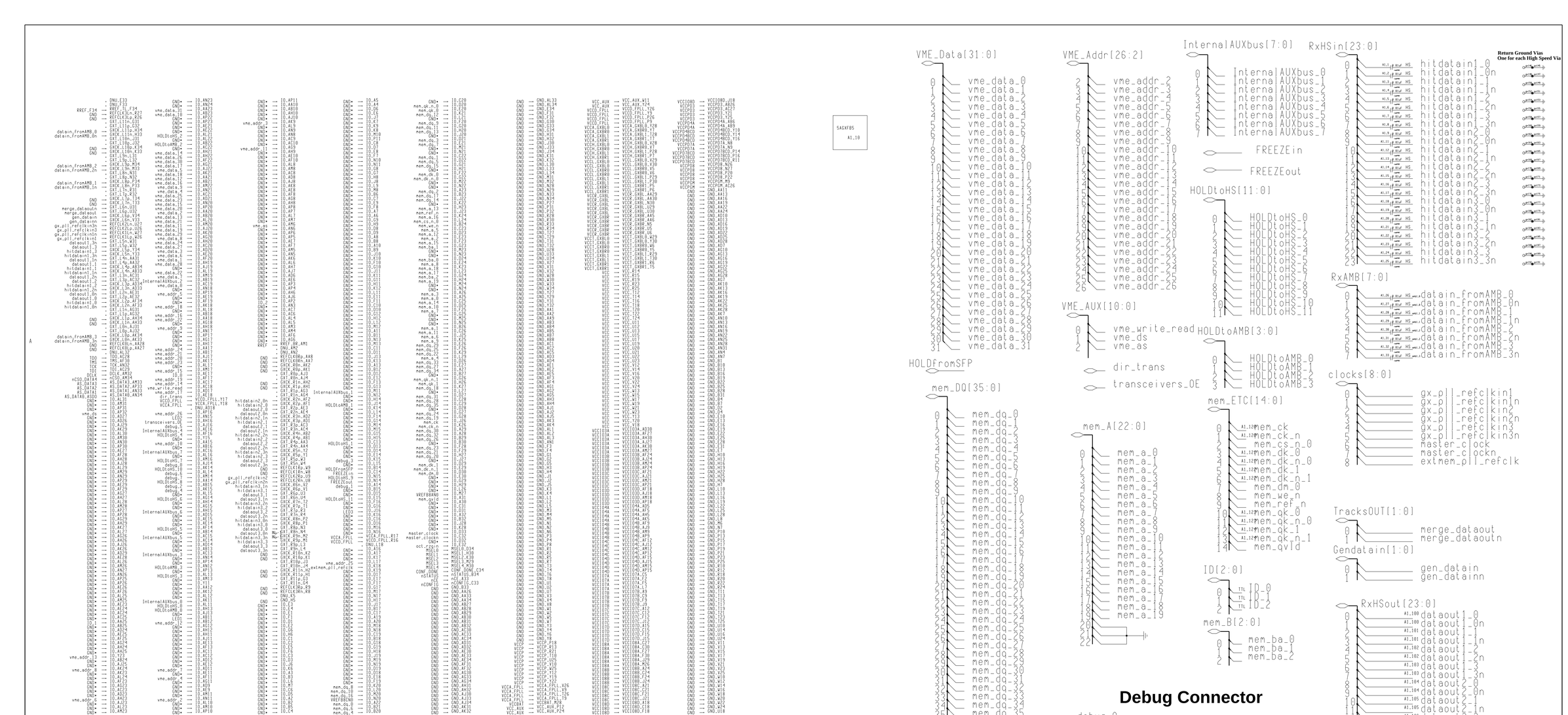
VME_Data[31:0]
VME_Addr[26:2]
InternalAUXbus[7:0]
RxHSin[23:0]
Return Ground Vias
One for each High Speed Via
SAGFXBS
A1_10
HOLDtoHS[11:0]
HOLDtoAMB[3:0]
HOLDfromSFP
mem_DQ[35:0]
mem_A[22:0]
mem_ETC[14:0]
VME_AUX[10:0]
FREEZEin
FREEZEout
ID[2:0]
mem_B[2:0]
RxAMB[7:0]
clocks[8:0]
TracksOUT[1:0]
Gendatain[1:0]
RxHSout[23:0]
Debug Connector
JTAG Connector
USB-Blaster
VCC_1.1V
VCCP_1.1V
VIO_3.0V
VIO_2.5V
VIO_1.8V
LR_GXB_1.15V
T_GXB_1.15V
VAUX_2.5V
H_GXB_1.5V
VREF_0.9V
GND*
2K A1_53 RREF
2K A1_531 RREF_F34
Sheet 22_1
Processor FPGA Decoupling
3.0V
RevB. Added resistor Ax_531
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 1/25/14
TIME: 9:17 am
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
Processor FPGA
FTK-AM-AUX Card
Size C
REV B
DRW. 2808
Sheet 20_1