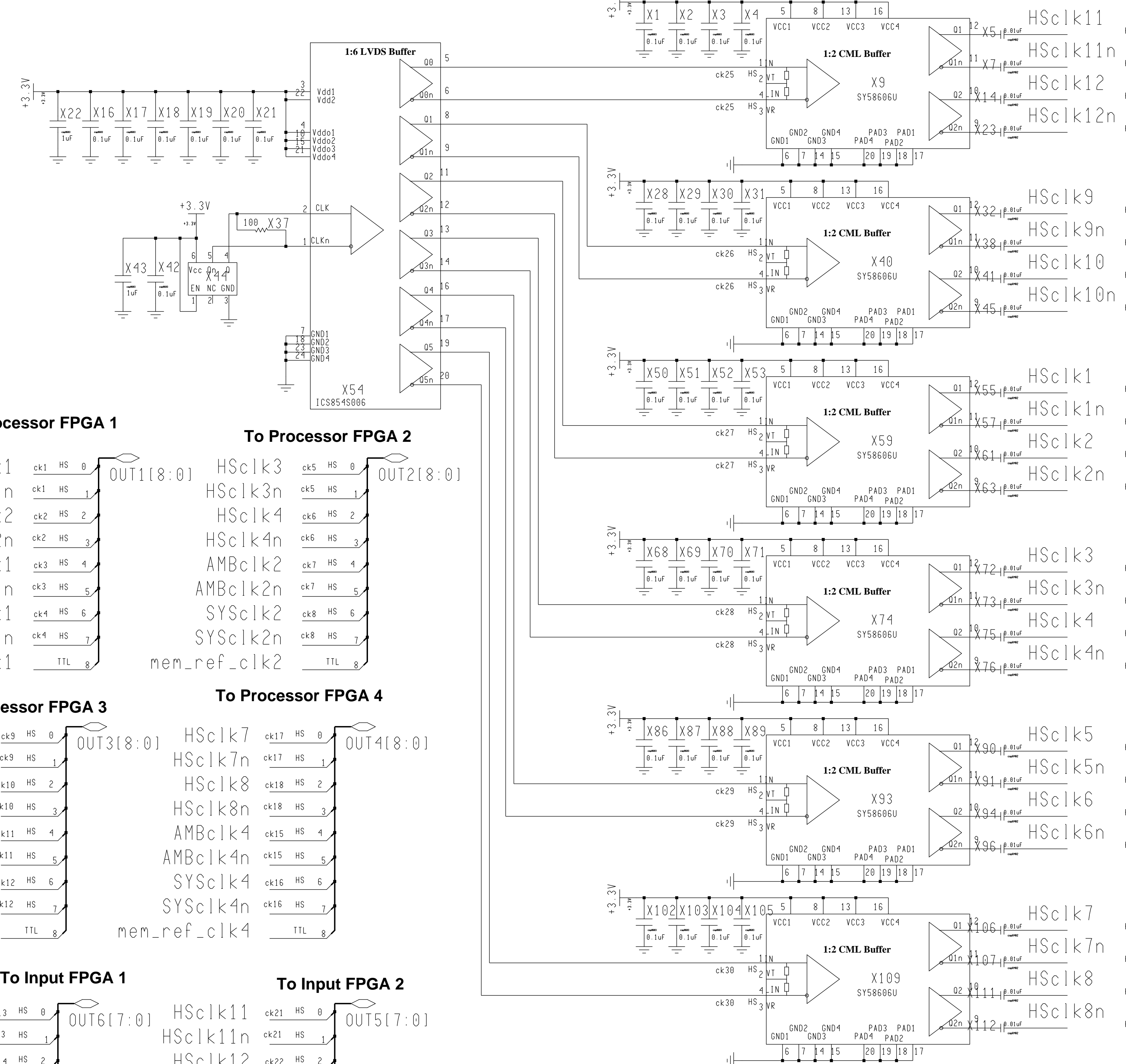


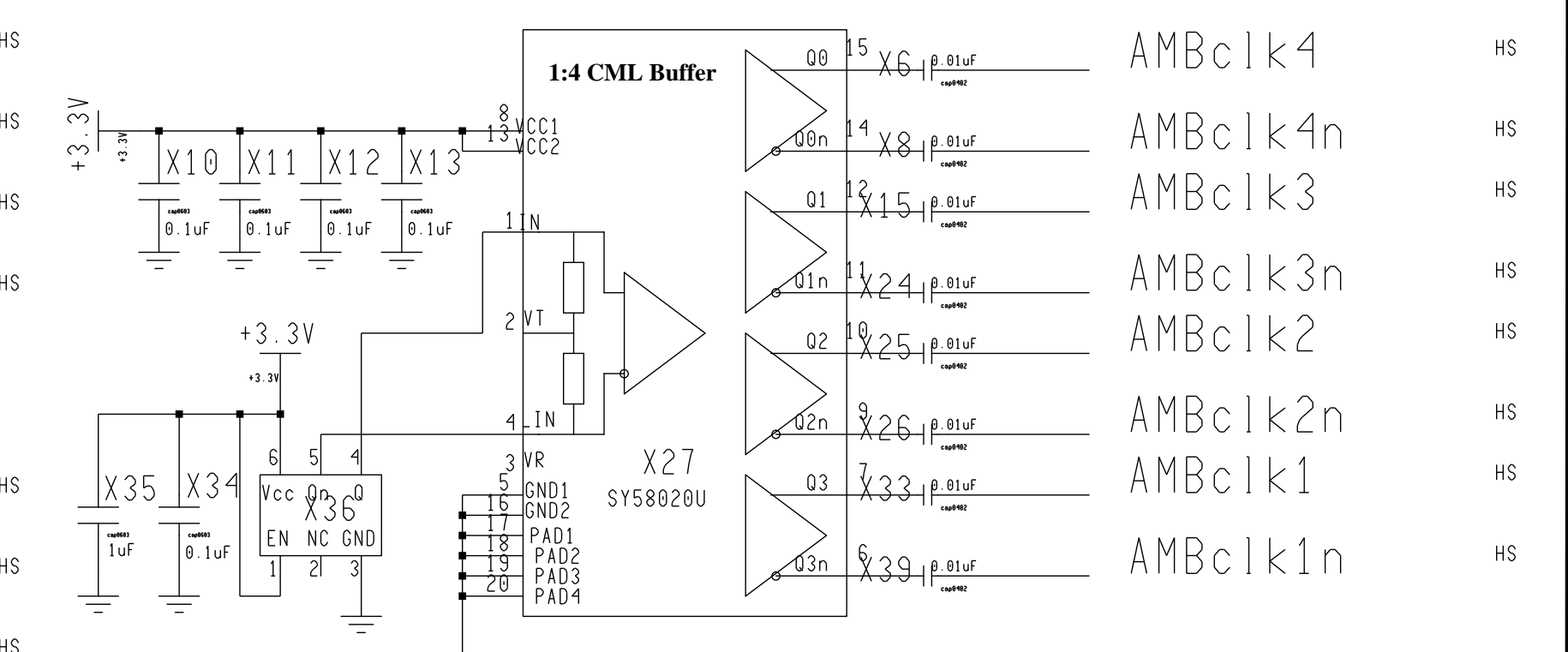
HS Reference Clock to all FPGAs

200MHz CML



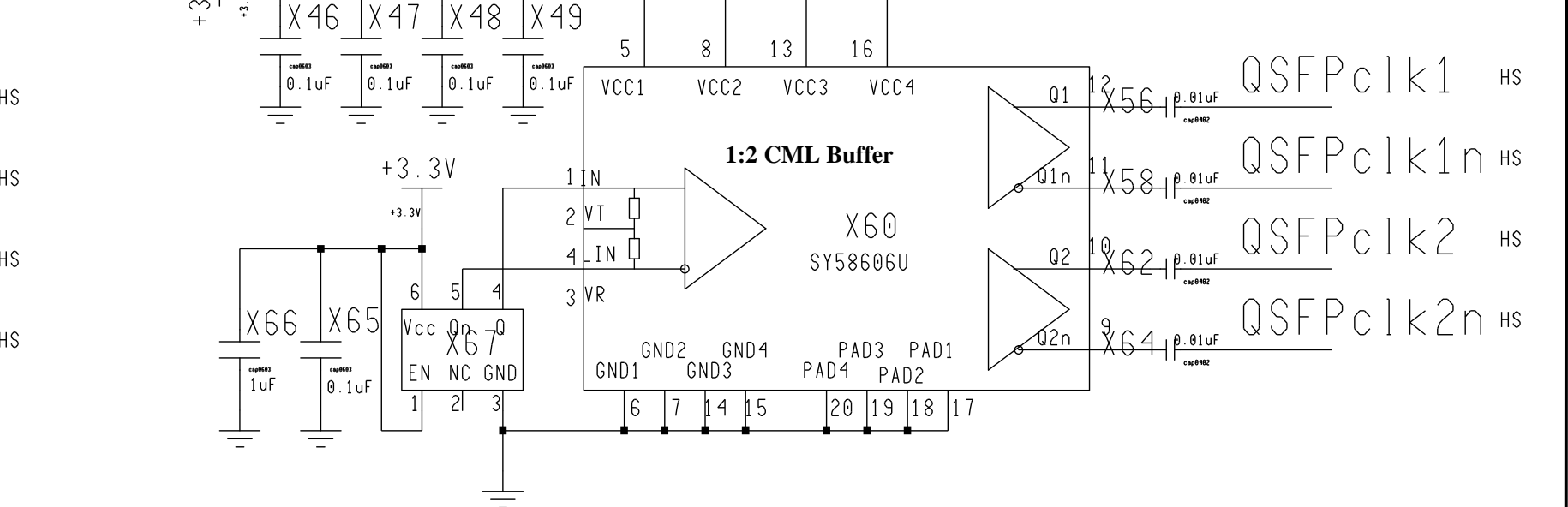
AMB Reference Clock to Processor FPGAs

100MHz CML



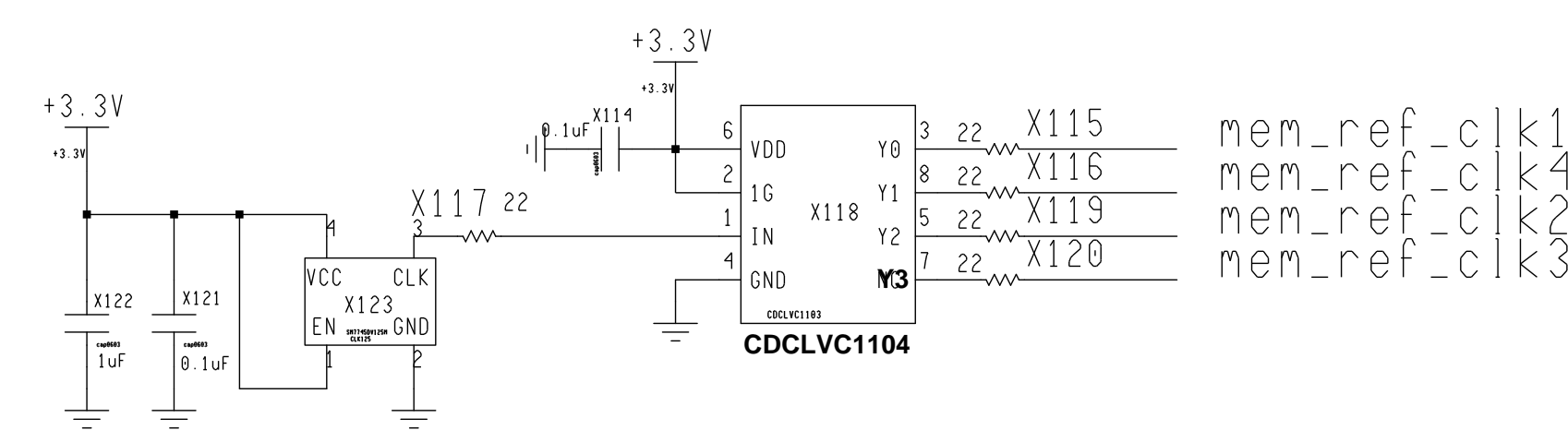
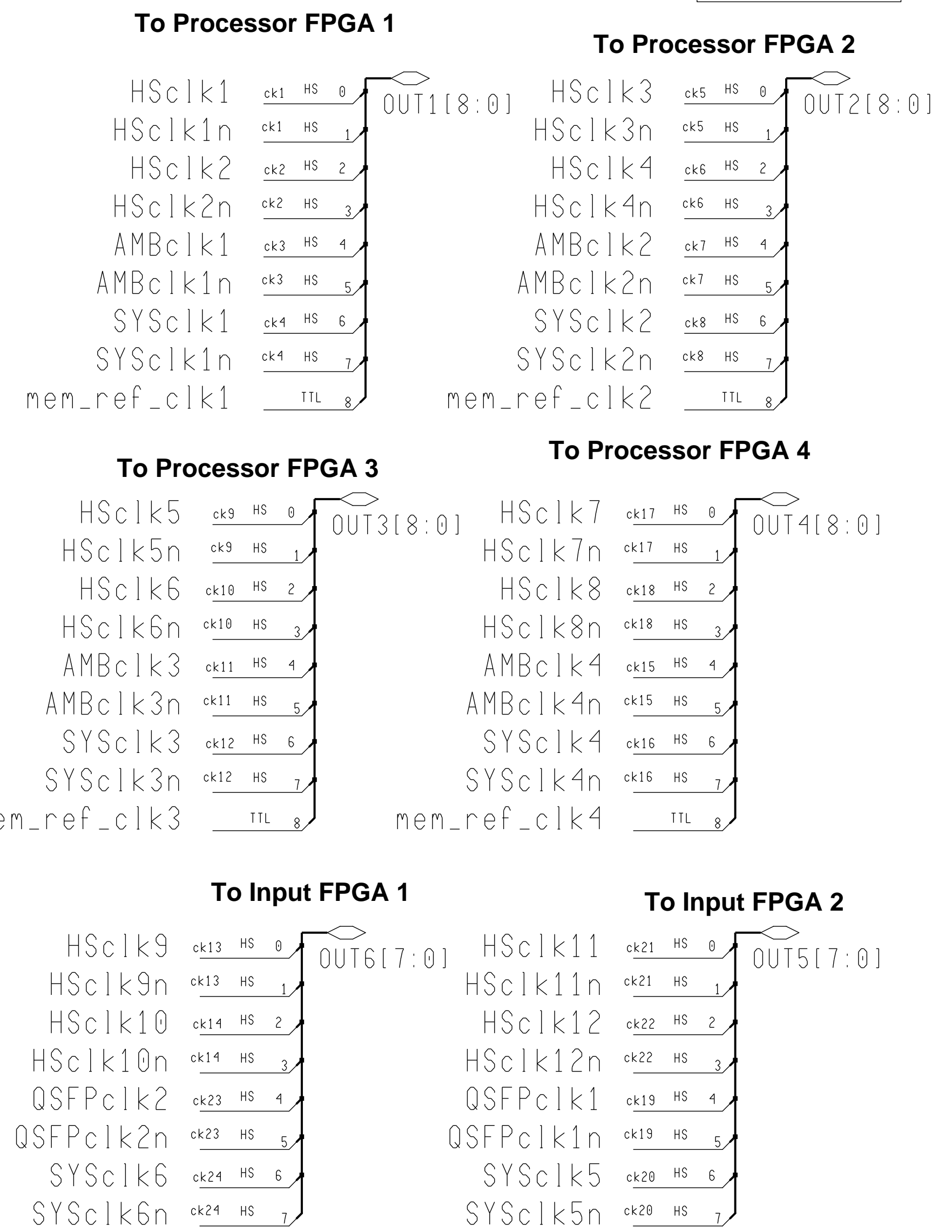
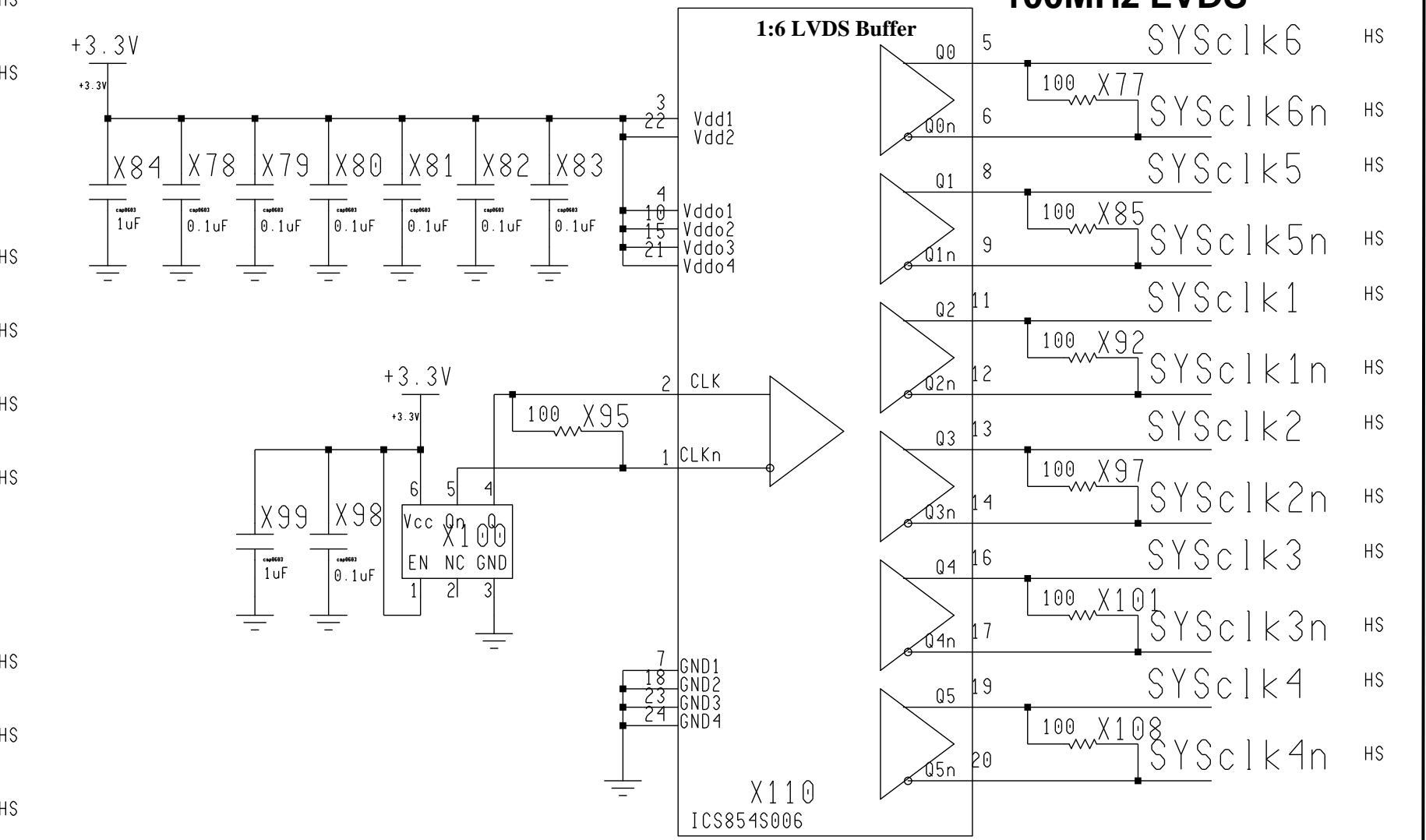
QSFP_Rx Reference Clock to Input FPGAs

200MHz CML



Internal Clock to all FPGAs

100MHz LVDS



Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE	Size c
DATE:	1/25/13	Clocks	
TIME:	10:17 am	FTK-AM-AUX Card	
REV	A	DRW.	2808
		Sheet	24