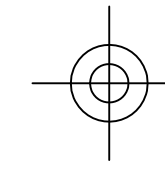
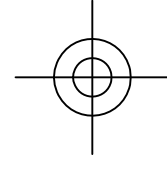
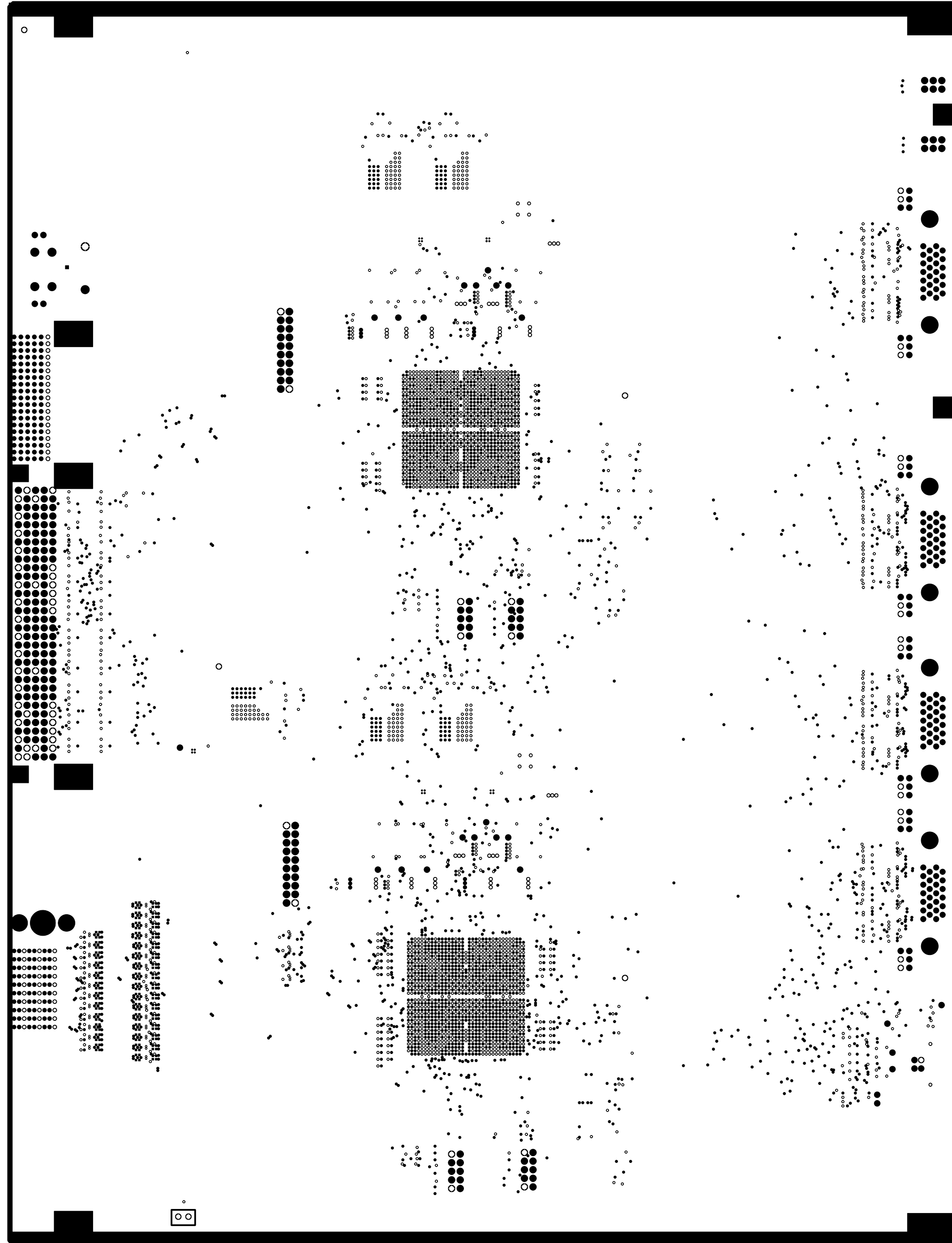
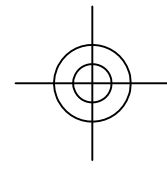


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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_1:Top: Signal_1

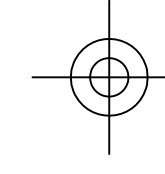


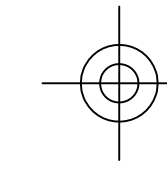
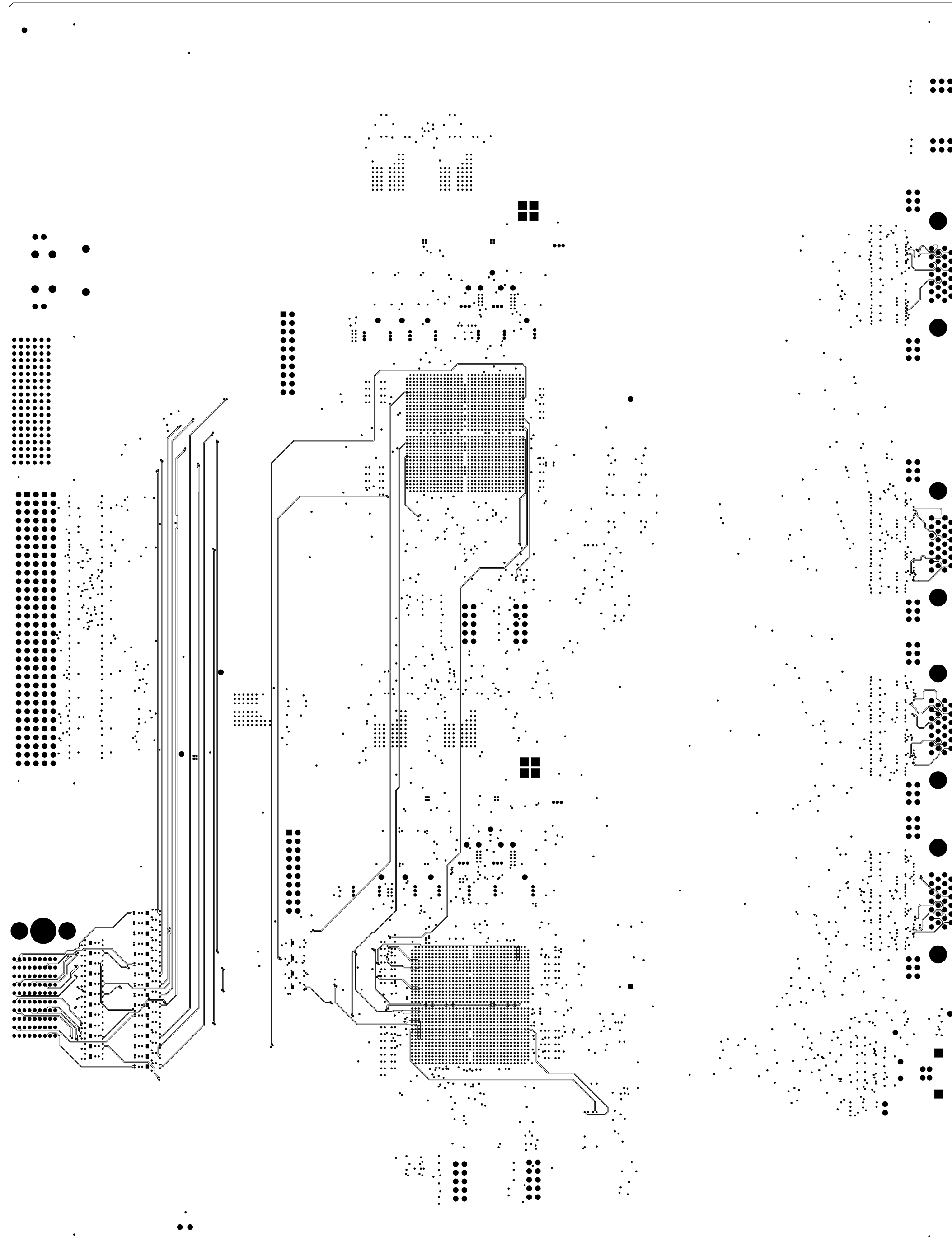
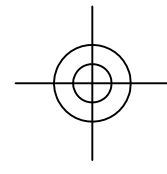
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Sch. Draw 2743 Rev A
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Asy. Draw 2745 Rev A

Artwork_2: Ground



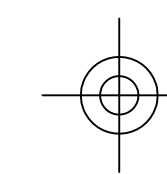
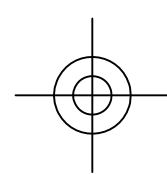


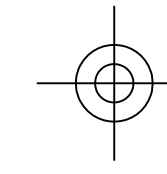
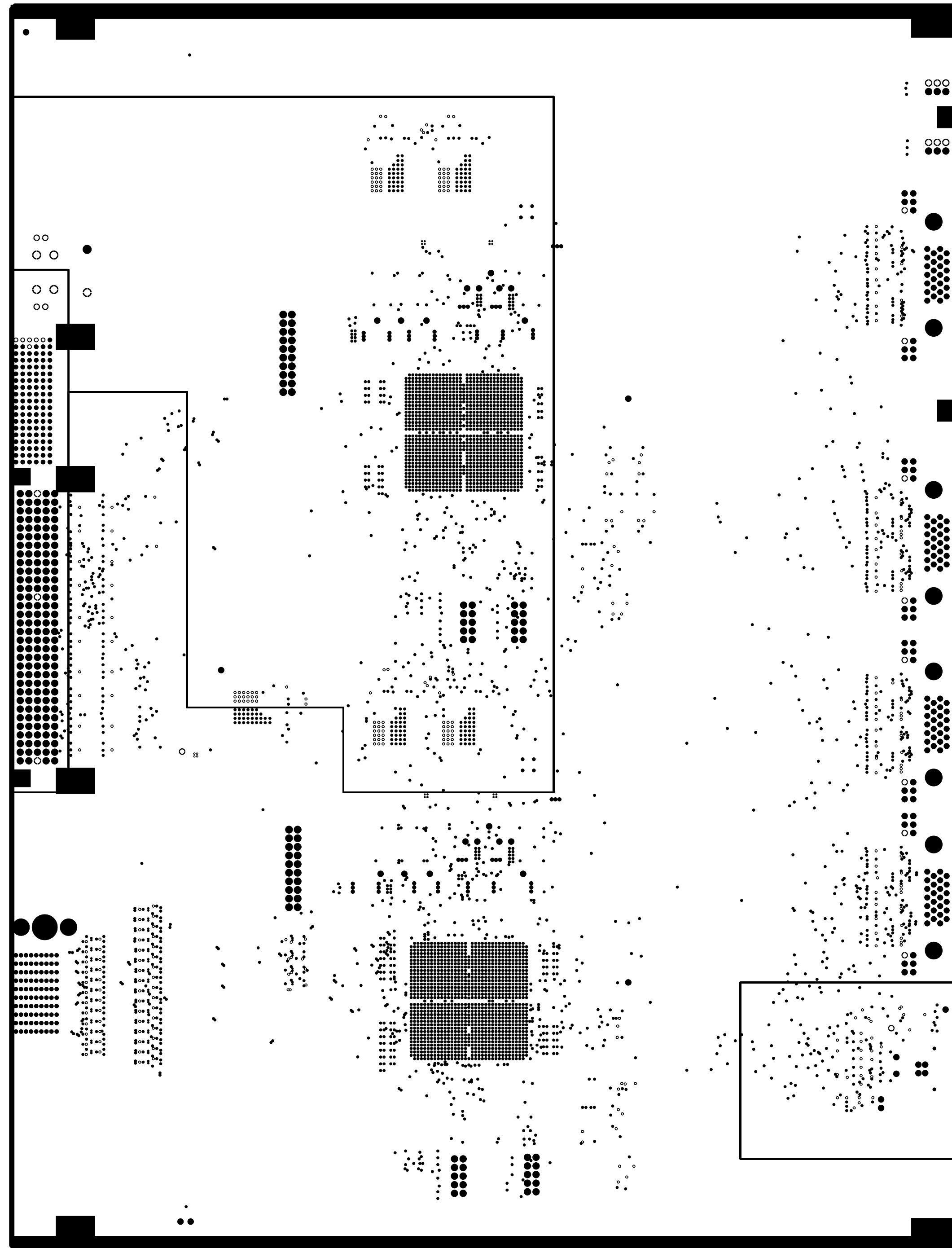
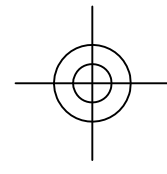
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_3: Signal_2



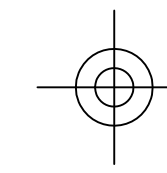
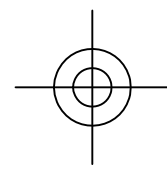


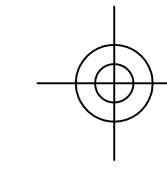
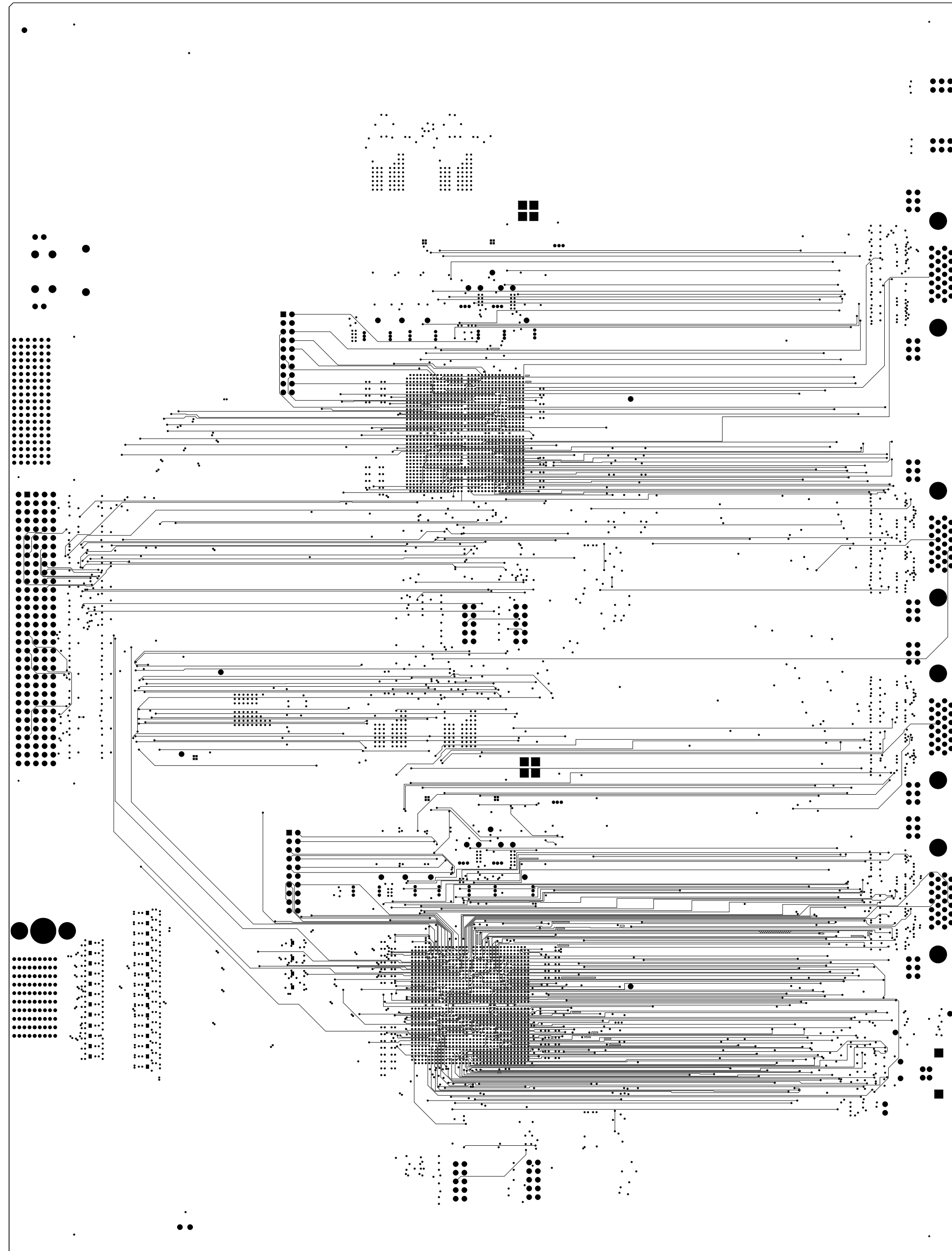
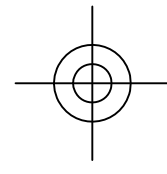
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_4: +5V, +3.3V, +3.3VUSB



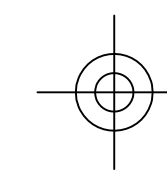
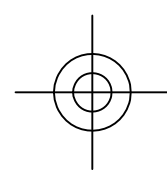


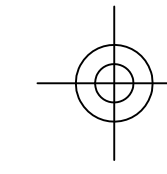
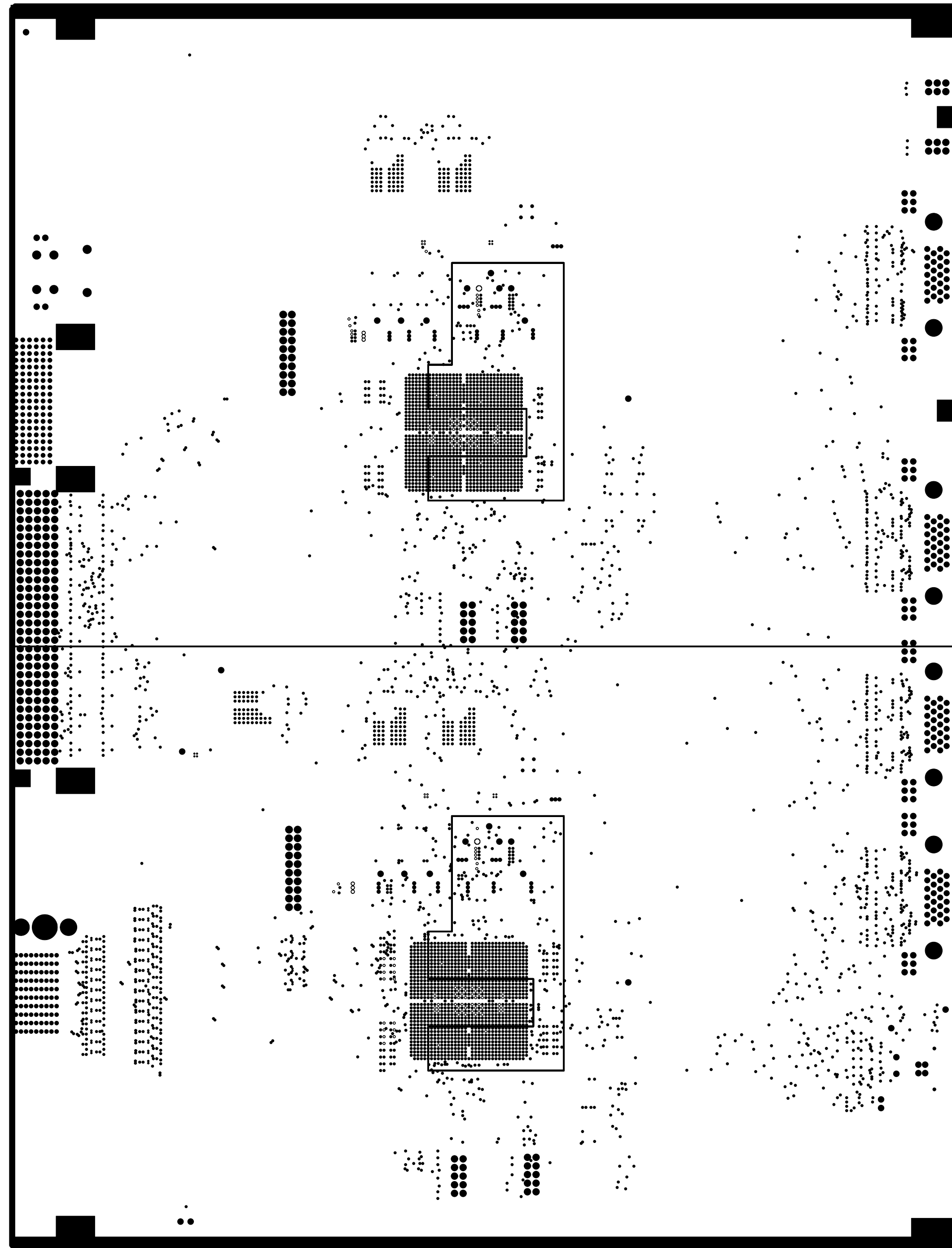
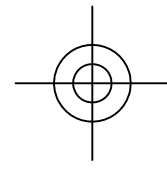
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_5: Signal_3



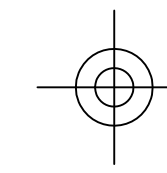
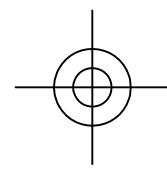


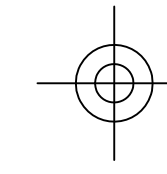
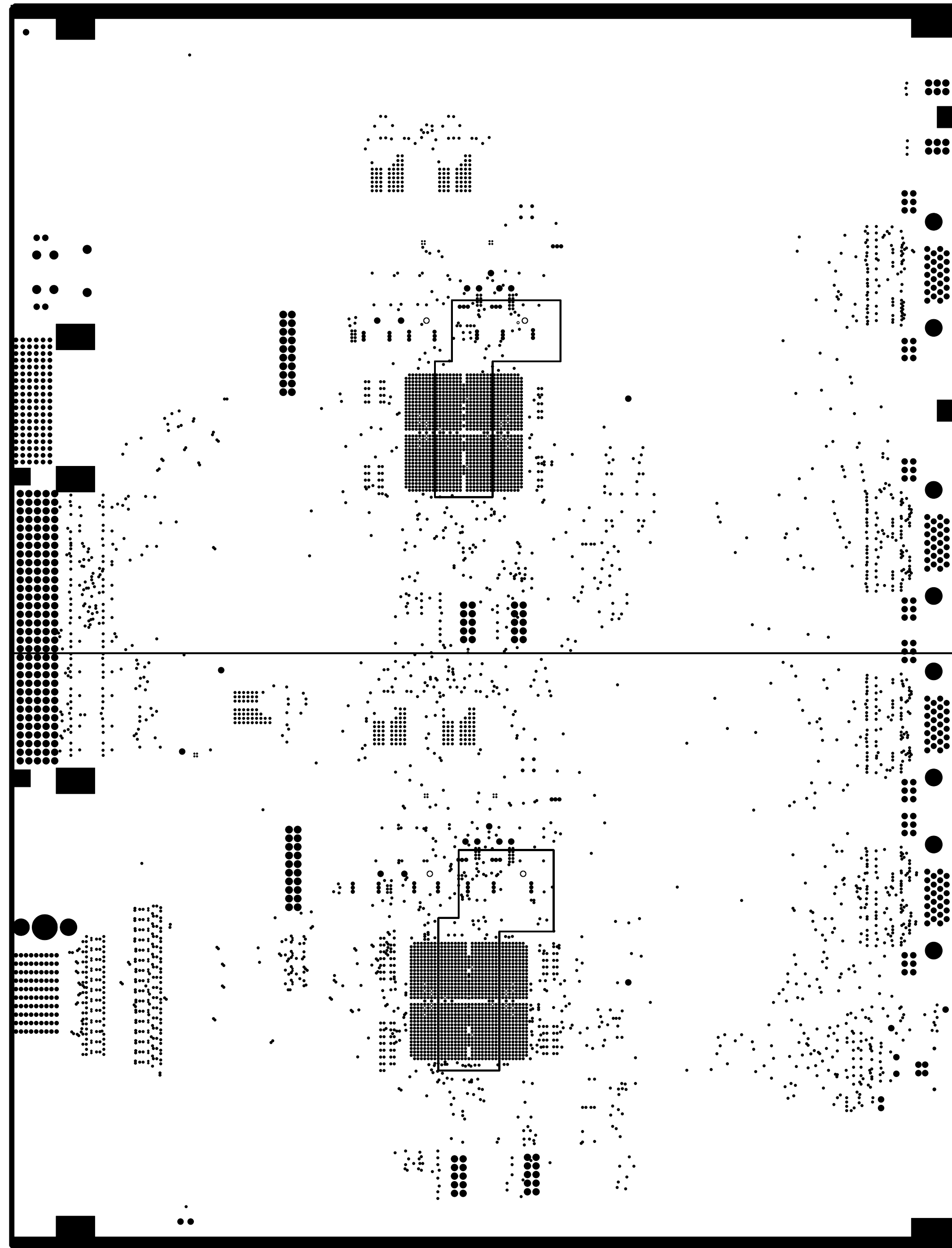
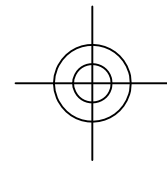
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_6: VCCR/TX, VCCAUXRX/TX



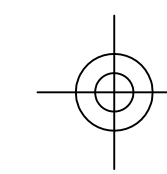
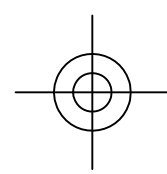


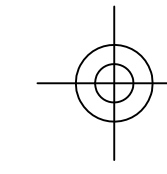
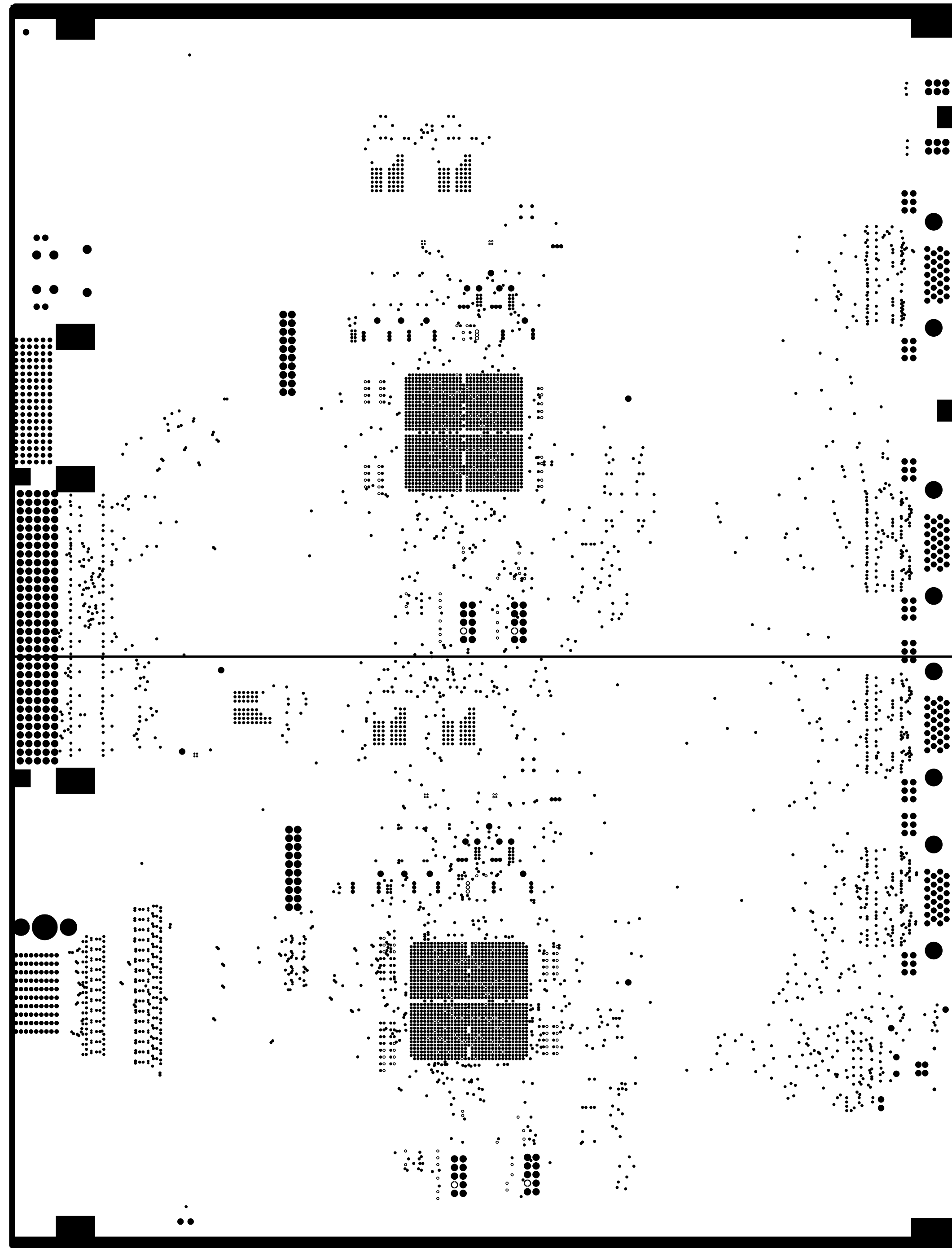
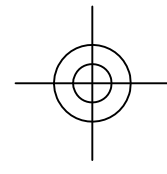
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Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_7: VCCD_PLLRX/TX, VCCRTL_LRGXBRX/TX



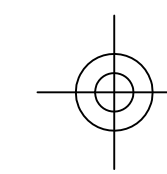
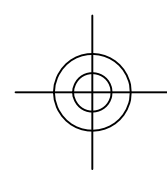


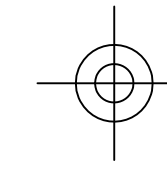
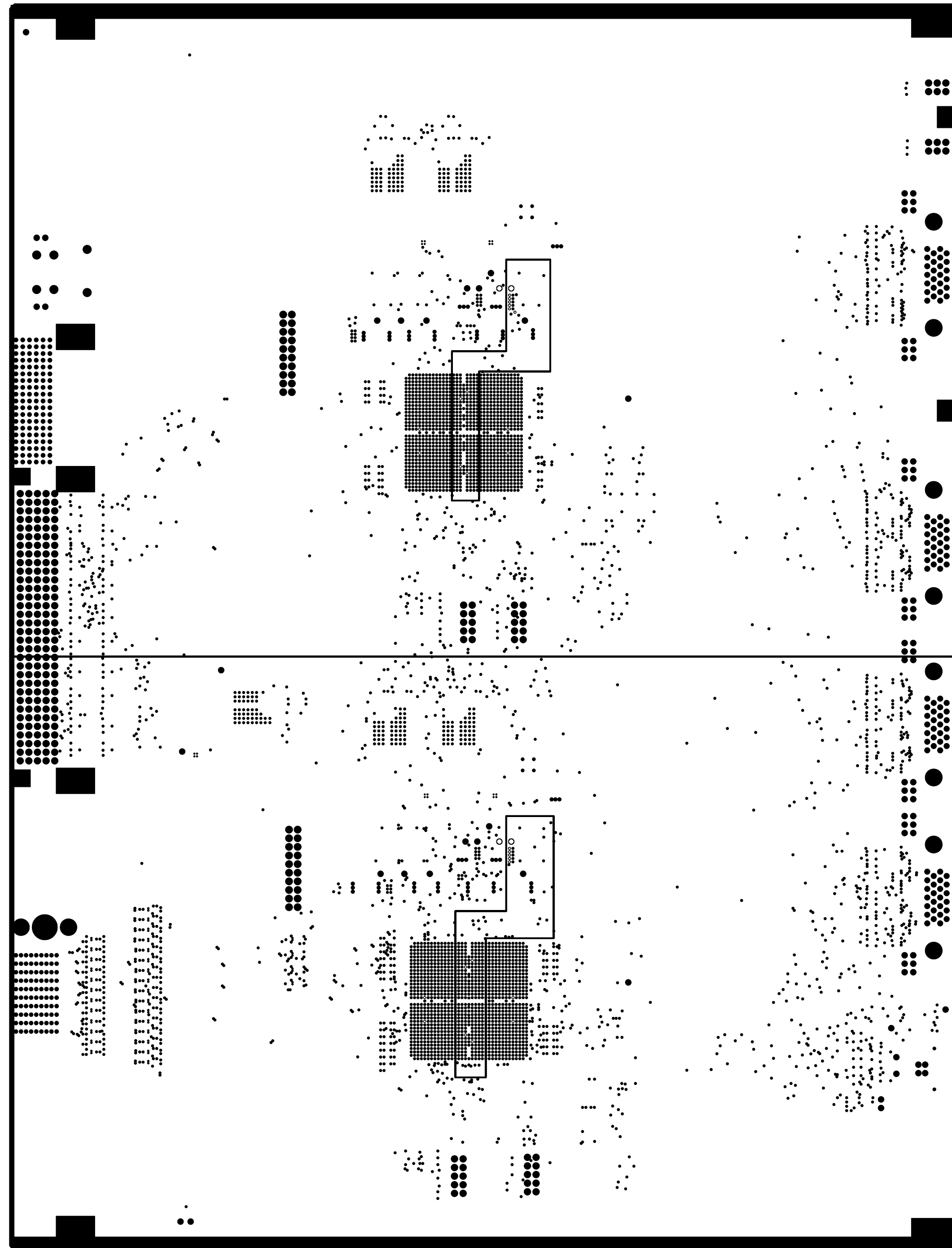
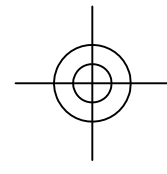
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Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_8: VCCI0RX/TX



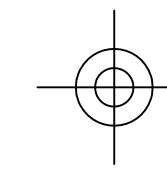
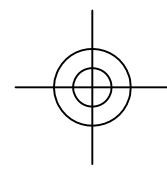


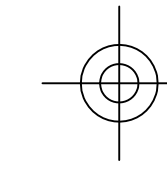
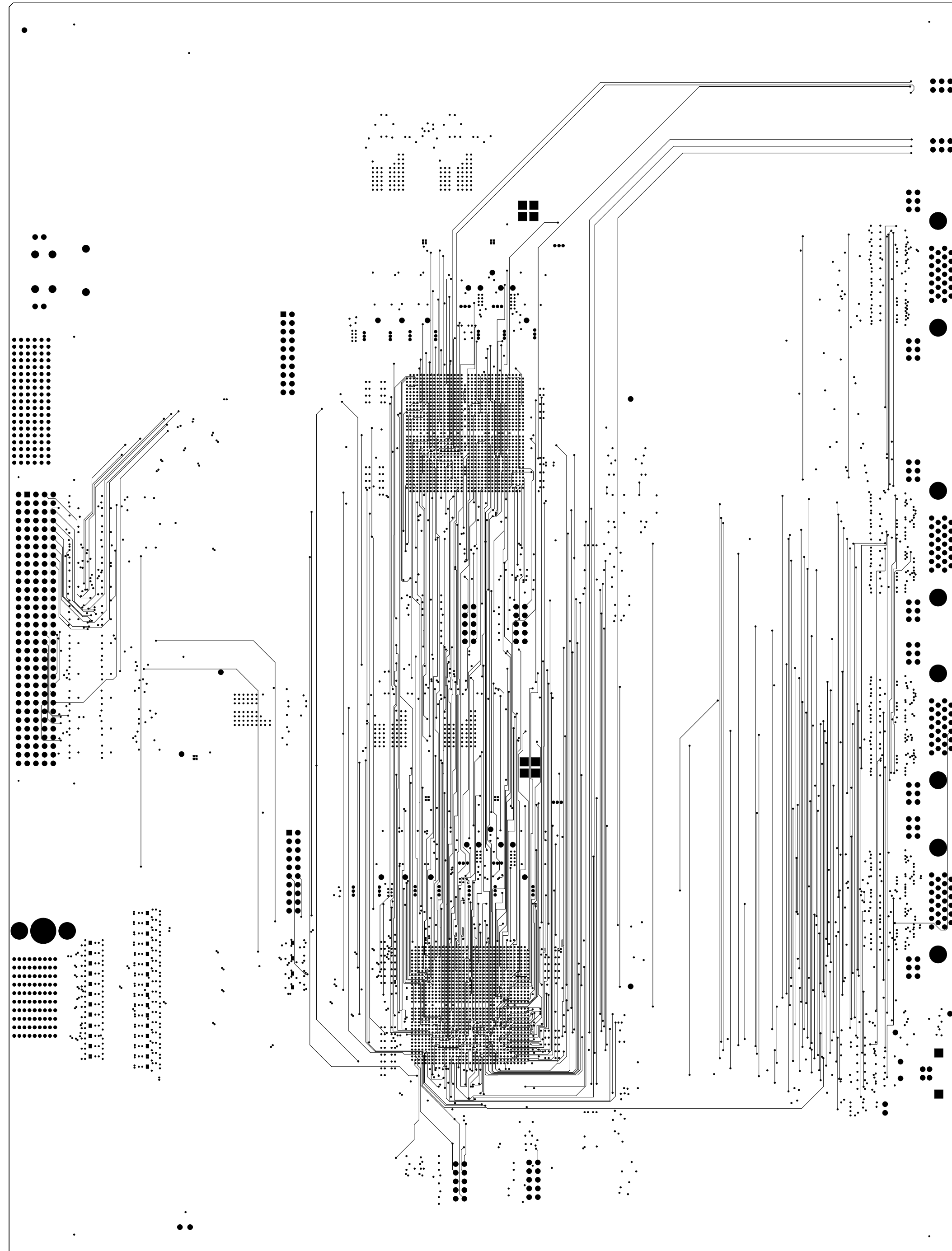
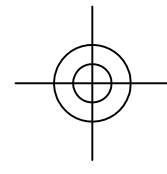
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_9: VCC_CLKINRX/TX, VCCA_LRRX/TX



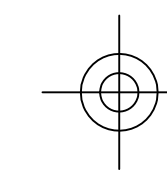
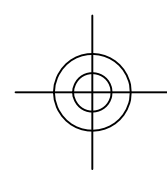


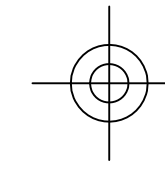
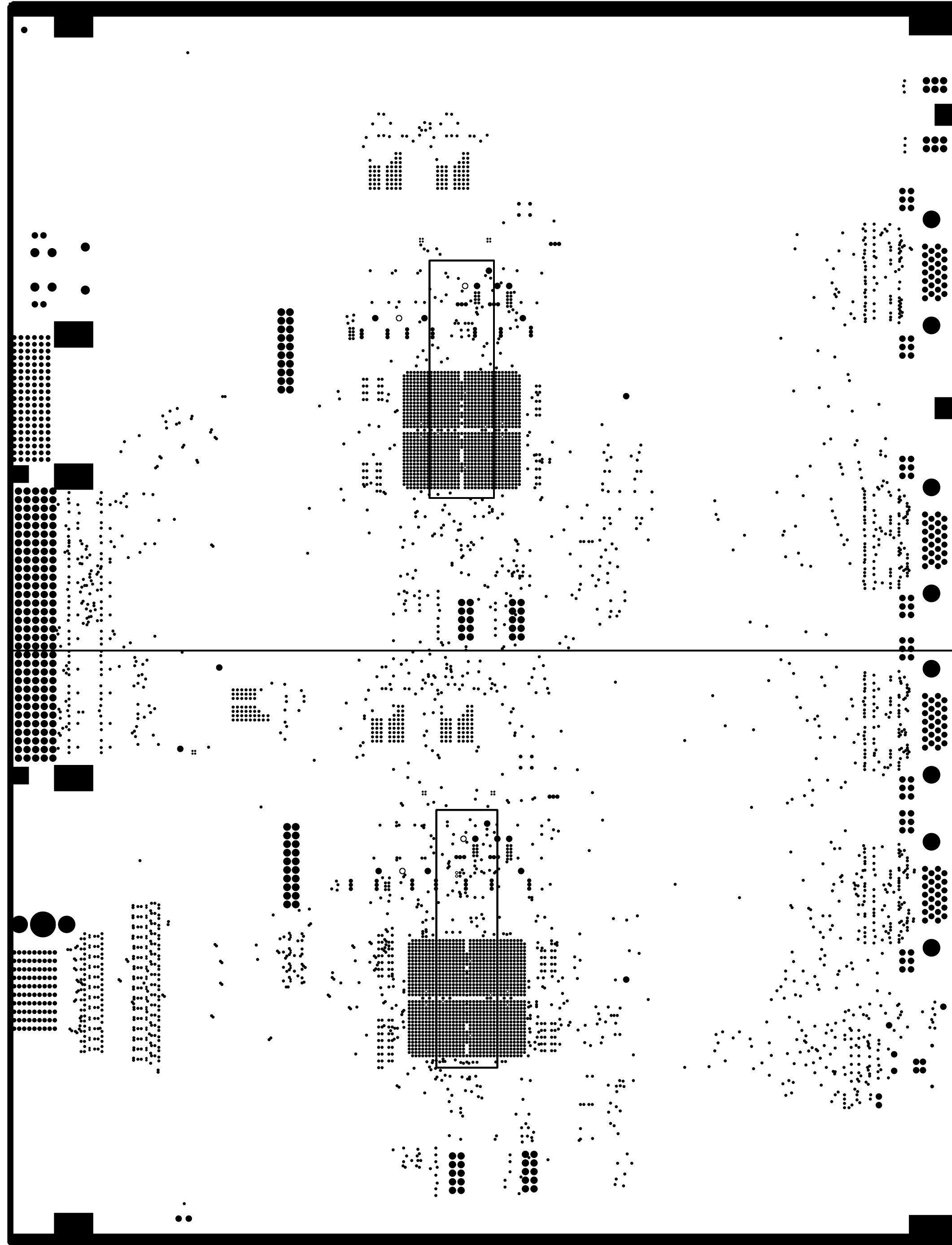
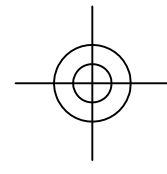
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_10: Signal_6



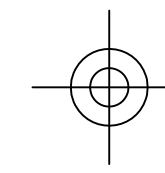
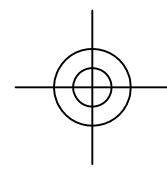


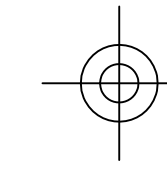
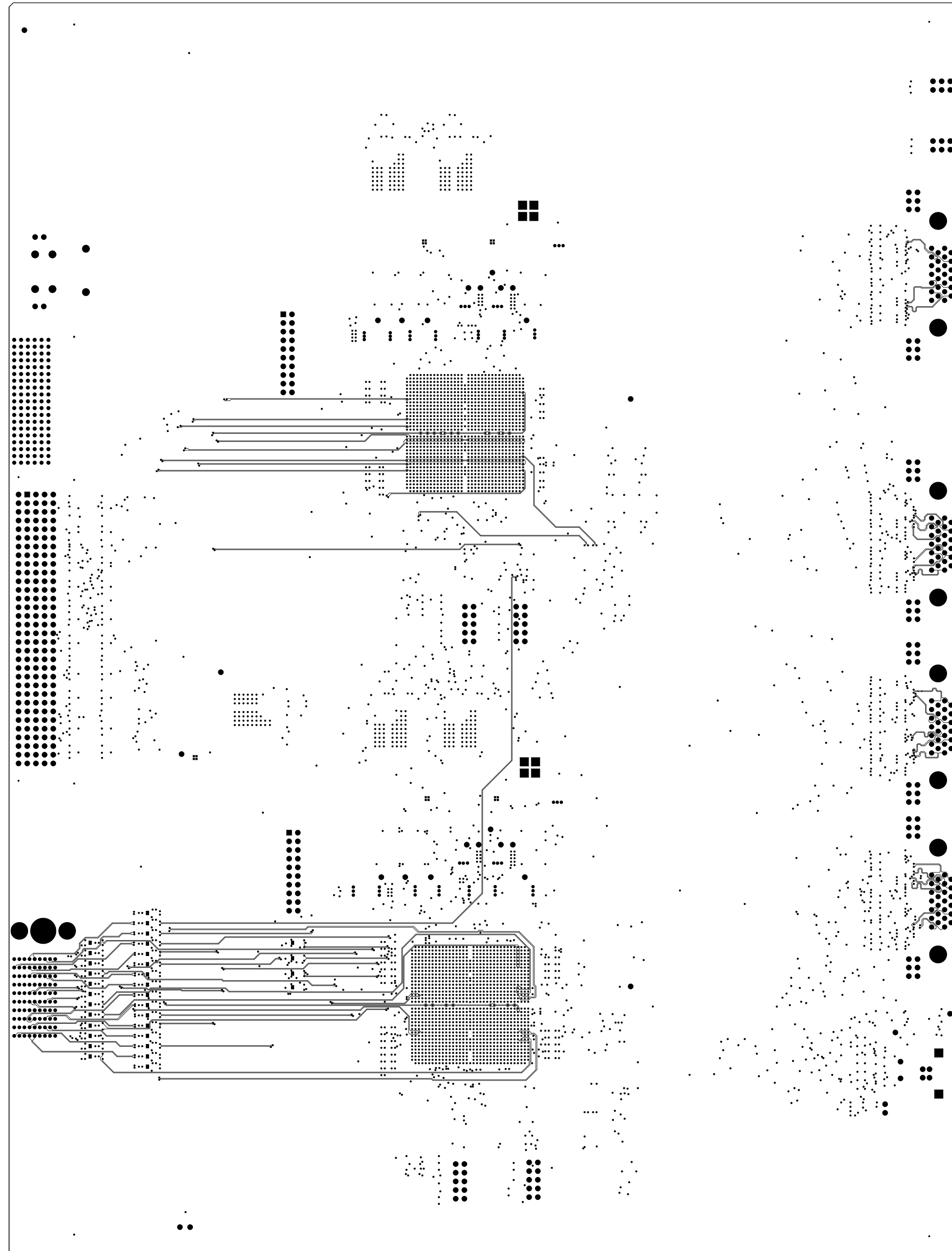
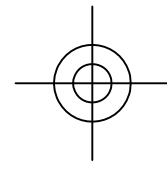
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_11: VCCA_PLLRX/TX. VCCH_GXBRX/TX



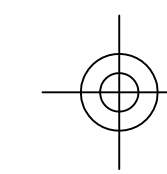
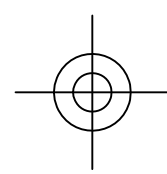


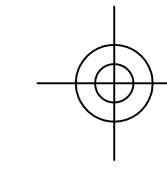
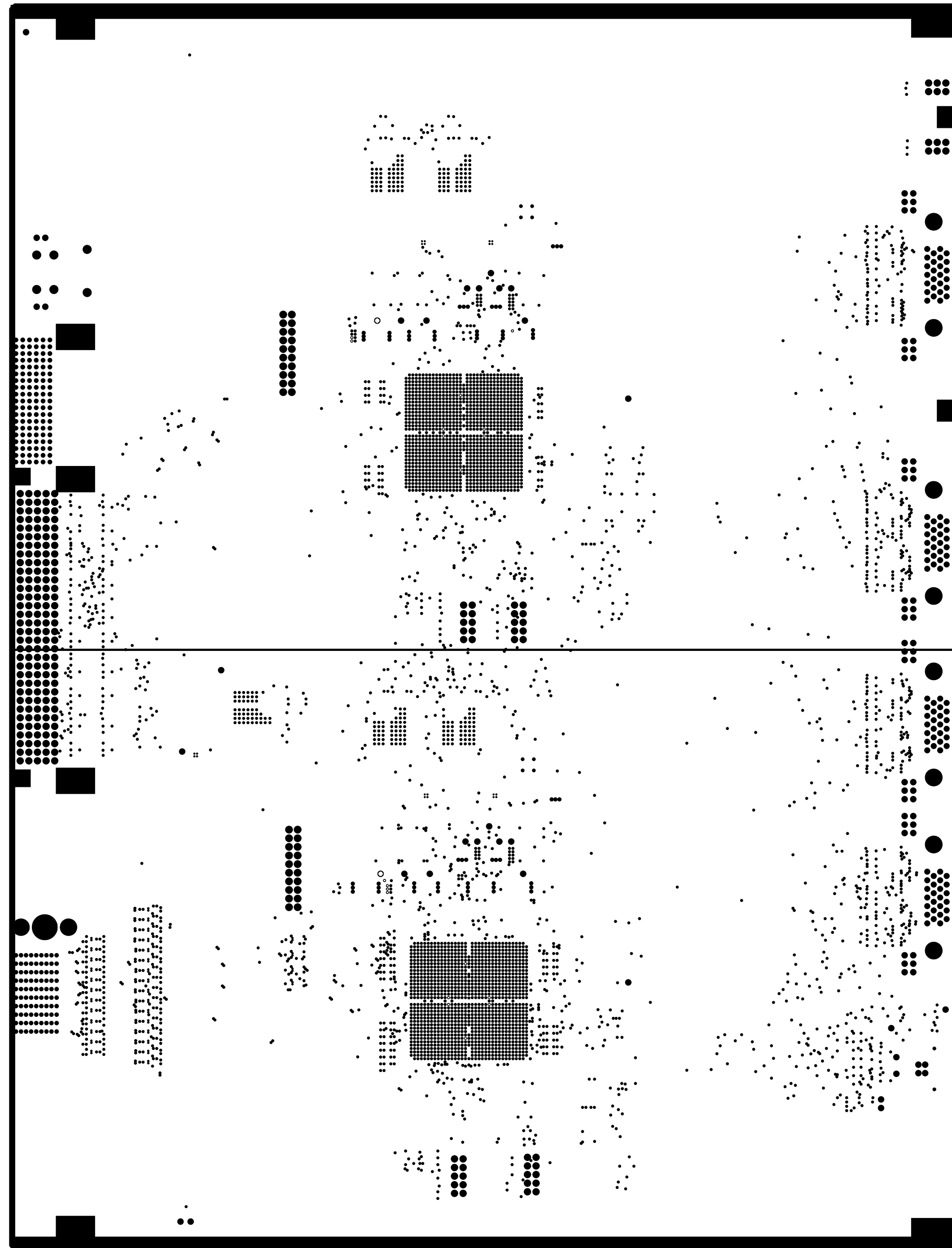
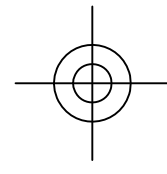
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_12: Signal_7



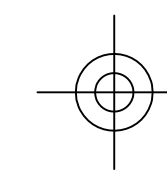
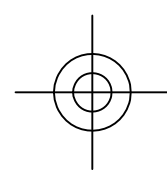


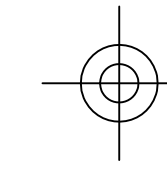
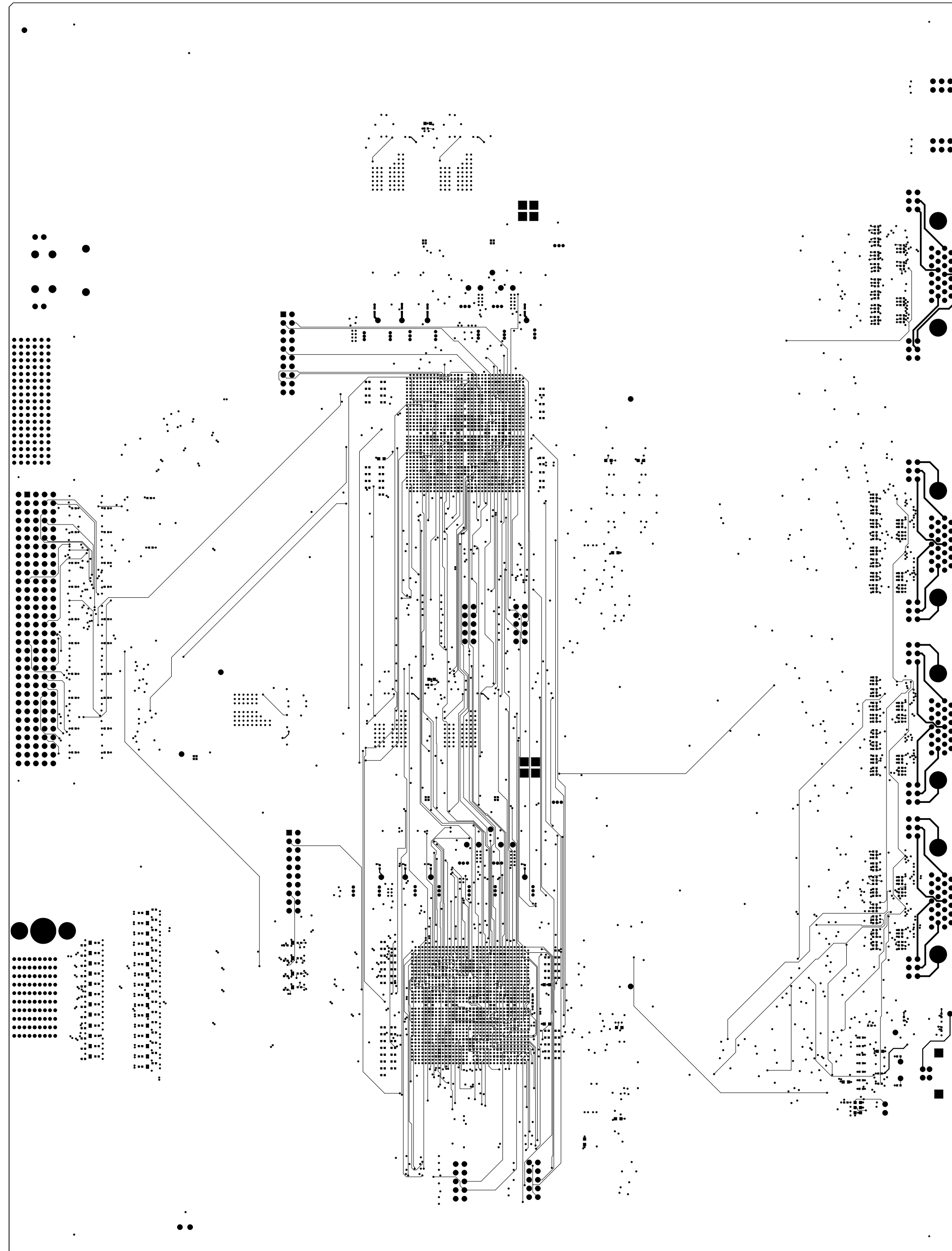
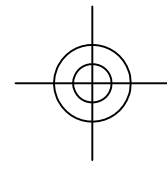
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_13: VCCPTRX/TX



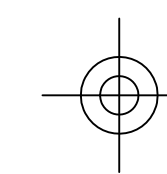
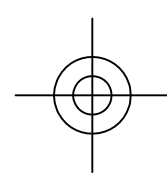


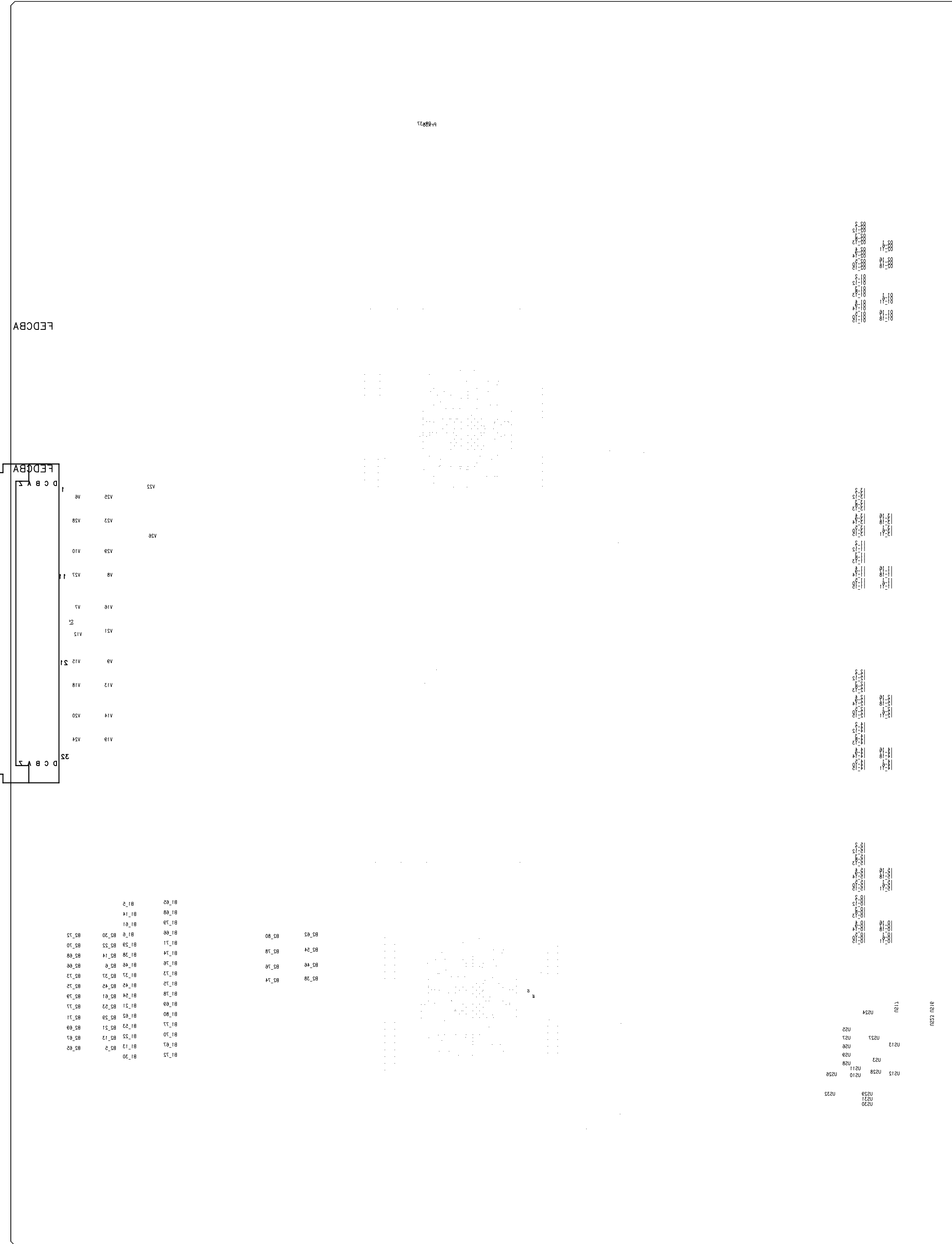
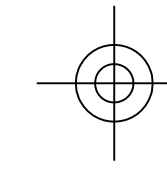
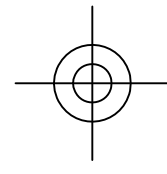
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Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_14: Signal_8, Bottom



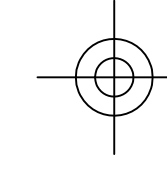
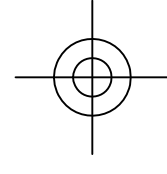


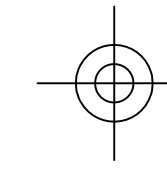
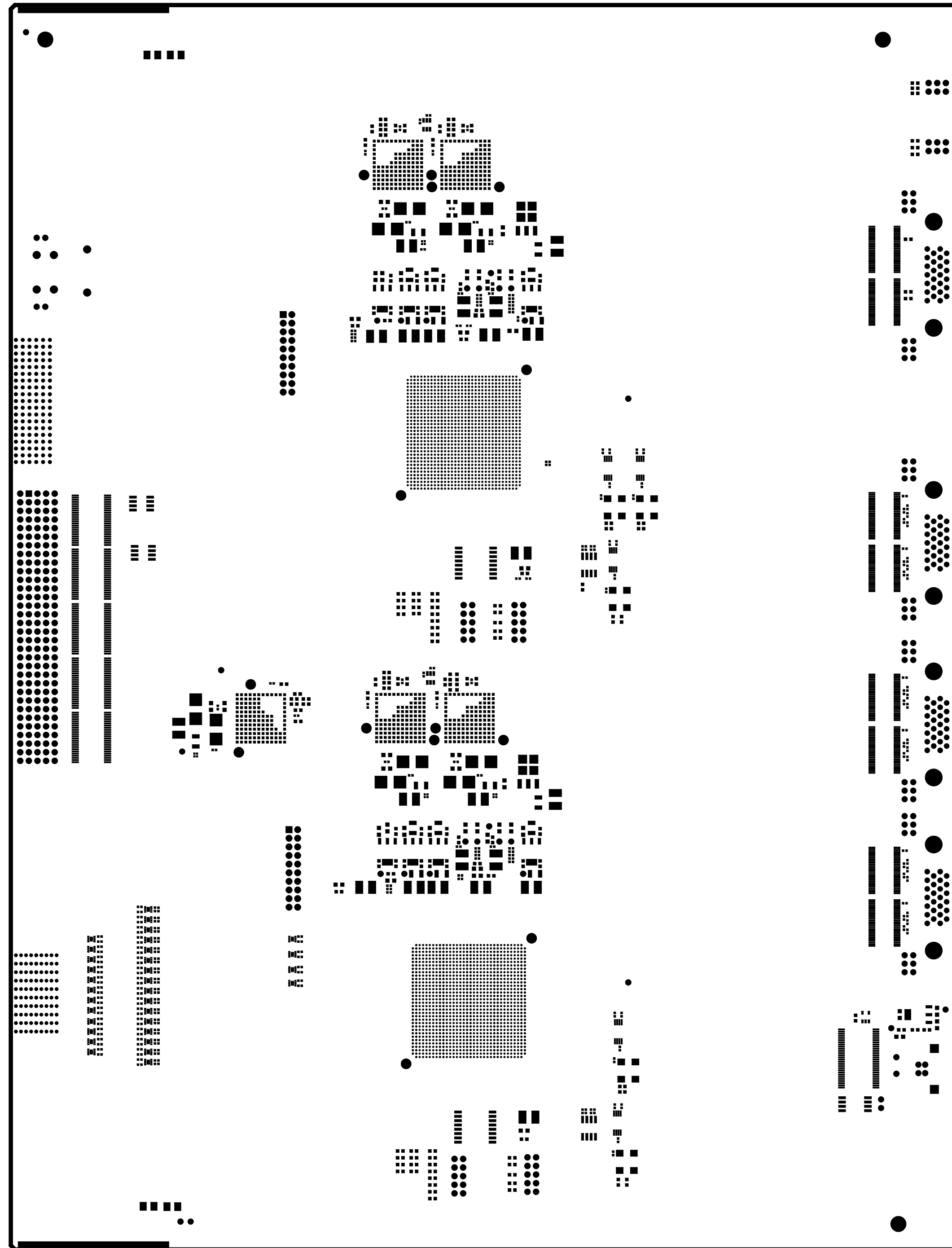
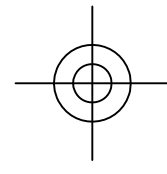
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Sch. Draw 2743 Rev A
 Spc. Draw 2744 Rev A
 Asy. Draw 2745 Rev A

Artwork_16: Bottom Silkscreen



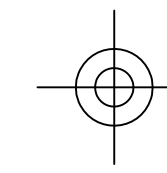
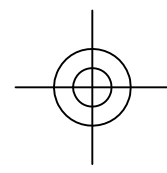


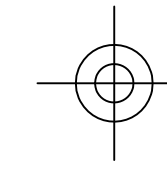
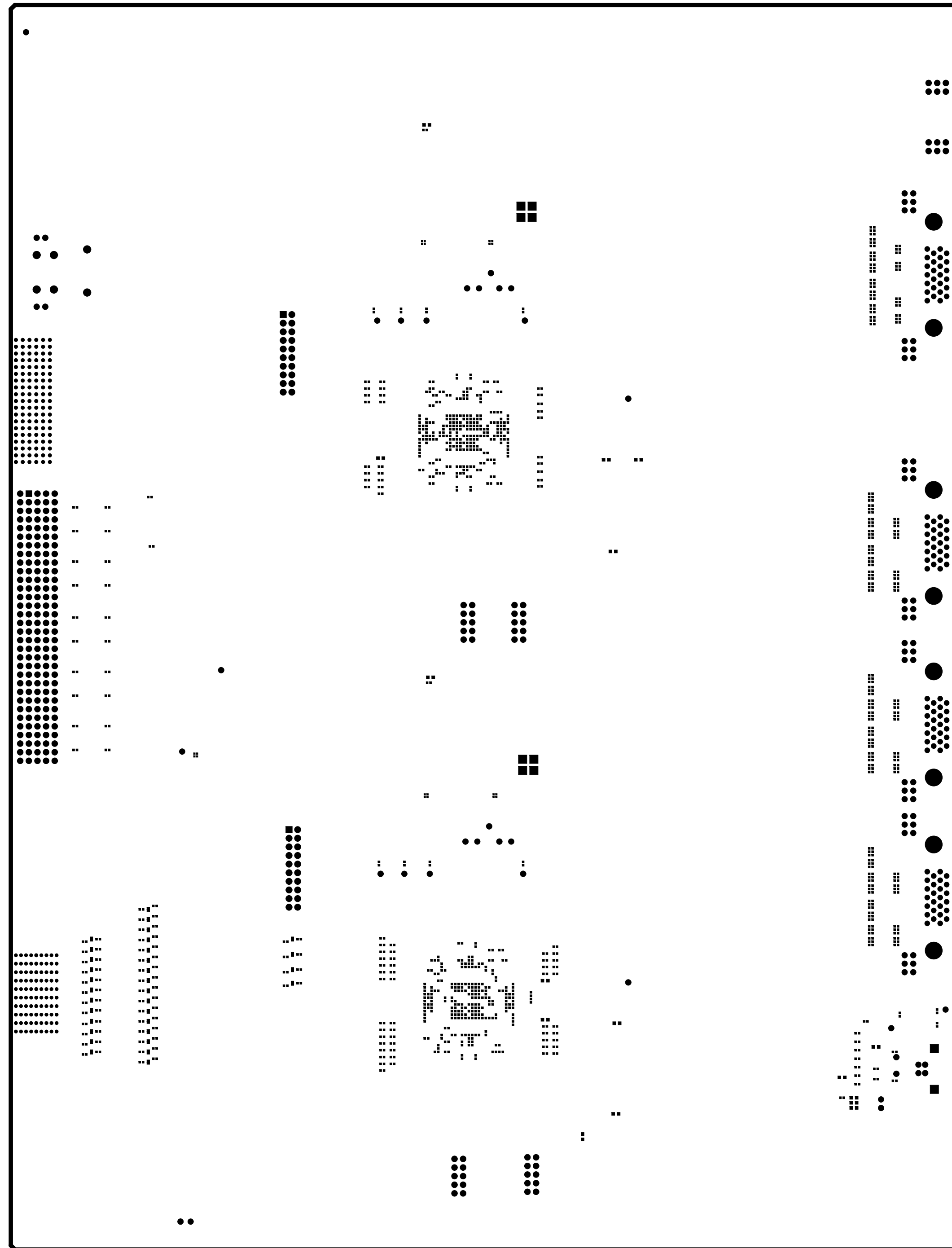
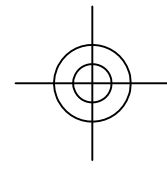
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Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_17: Top Soldermask



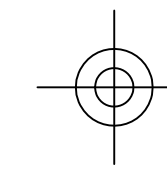
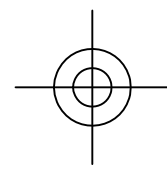


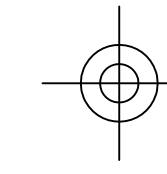
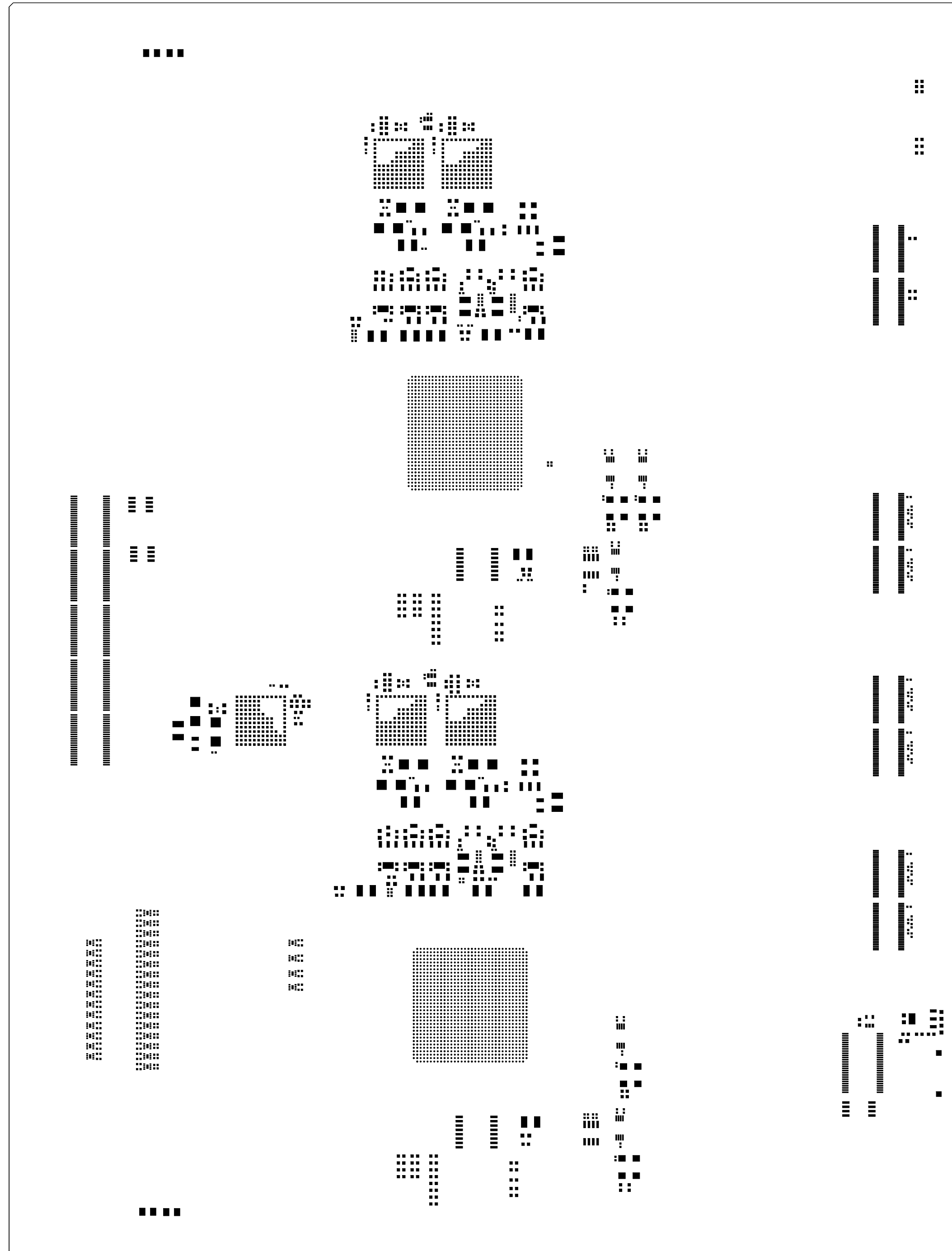
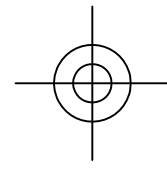
FTK Rear VME Test Card
Sept. 26, 2011

Mircea Bogdan
Electronics Design Group
University Of Chicago

Sch. Draw 2743 Rev A
Spc. Draw 2744 Rev A
Asy. Draw 2745 Rev A

Artwork_18: Bottom Soldermask



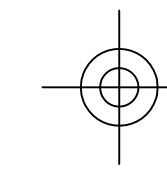
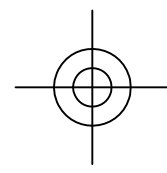


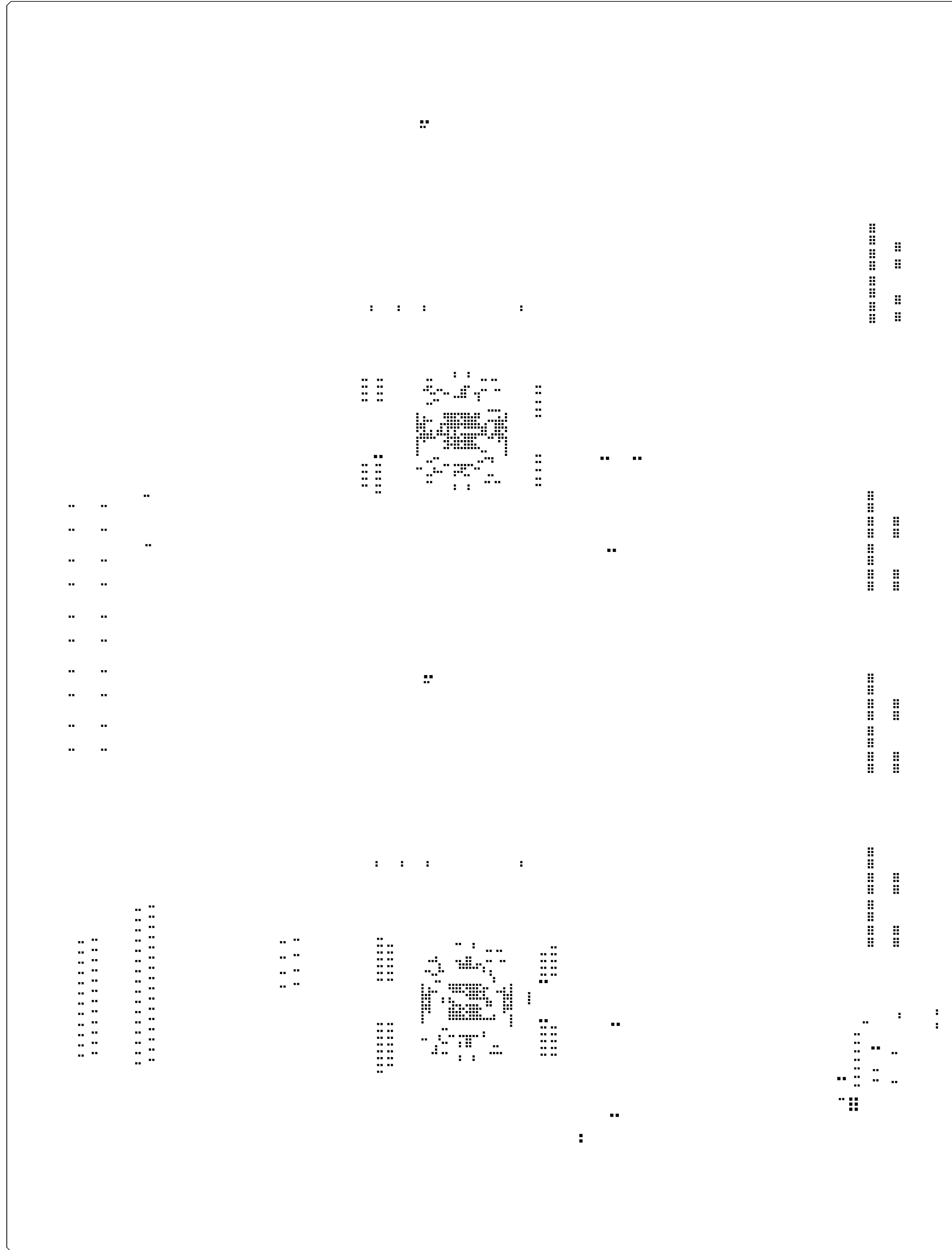
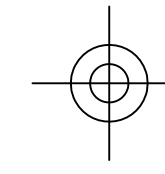
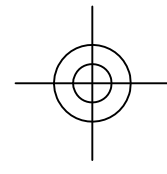
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Sch. Draw 2743 Rev A
 Spc. Draw 2744 Rev A
 Asy. Draw 2745 Rev A

Artwork_19: Top Pastemask





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Sch. Draw 2743 Rev A
 Spc. Draw 2744 Rev A
 Asy. Draw 2745 Rev A

Artwork_20: Bot Pastemask

