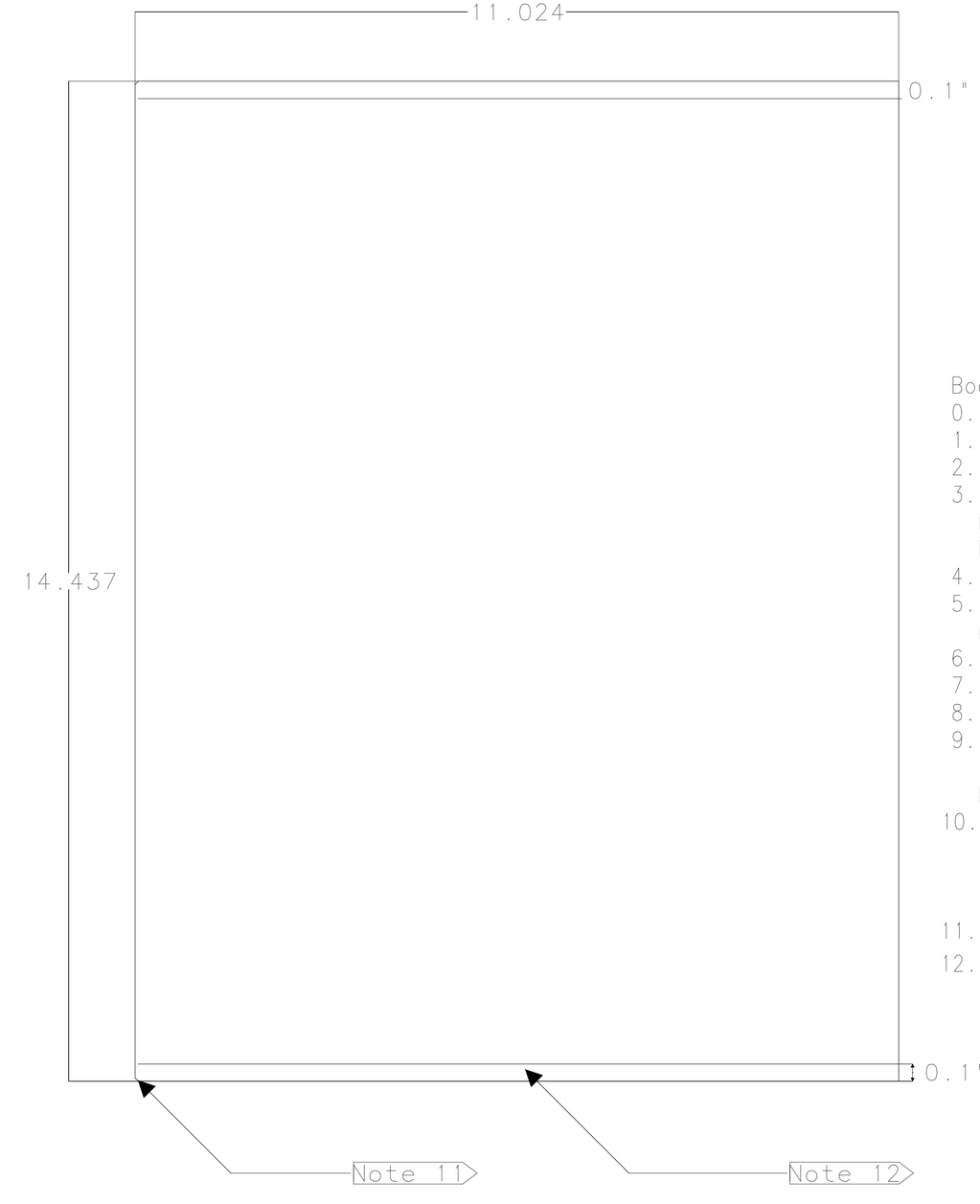
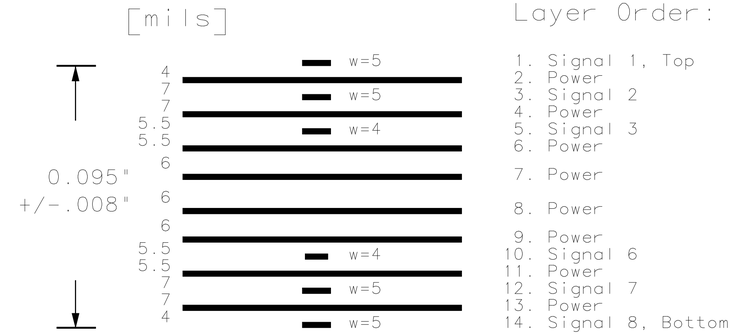
DWG.NO. 2744 | SH 1 | REV. A



BOARD's HOLE SCHEDULE

FHS	COUNT	PLATED	COMMENT
.009	4998	YES	
.012	94	YES	
.02	60	YES	
.0236	204	YES	Note 10
.03	104	YES	
.035	6	YES	
.041	333	YES	
.057	6	YES	
.106	8	NO	
.11	8	YES	
.113	5	NO	
.122	2	NO	
.2165	1	NO	



Board Characteristics: 14-Layer Board

0. All dimension in inches unless specified otherwise.
1. Material: FR4, Tg > 170 C.
2. Board Thickness: 0.095"+/-0.008"
3. Minimum Trace Width 0.005" on Layer 1,3,12,14
   Minimum Trace Width 0.004" on Layer 5,10
   Minimum clearrence 0.004" on all layers.
4. 1 oz Copper for top, bottom and power layers; 1/2 oz Copper for embedded signal layers.
5. Electroless Nickel/Immersion Gold plating; apply solder mask.
   min 25 um Cu, 2.5-5 um Ni, 0.05-0.2 um Au (Electroless Ni/Immersion Au).
6. Silkscreen on Both Sides
7. Interlayer spacing : as specified.
8. FHS tolerances : +/- 0.002" unless specified otherwise.
9. Impedance 50 Ohm for all 5-mil traces on Layers: 1,3,12,14
   Impedance 50 Ohm for all 4-mil traces on Layers: 5,10
   Present TDR test results for all signal layers.
10. This is a pressfit tech. thru hole with the following specs:
    - Diameter of drilled hole: 0.7mm +/-0.02mm
    - Diameter of finished plated through hole: 0.6 mm +/-0.05mm
    - Hole Plating: min 25 um Cu, 2.5-5 um Ni, 0.05-0.2 um Au (Electroless Ni/Immersion Au).
11. 45 degree chamfer
12. Mill the Top and Bottom of Board on the SIder Side to a thickness of 0.063" +/- 0.008".
    Width of the milled areas: 0.1" +/- 0.05"

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.008
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M. Bogdan	9/22/11
CHECKED H. Sanders	9/22/11
ISSUED	

THE UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE FTK VME Test Aux Board Specification Drawing

SIZE | FSCM NO. | DWG. NO. 2744 | REV. A

SCALE 1/2 | SHEET 1 of 1

THIS SHEET IS COMPUTER GENERATED