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| Engineer | M. Bogdan | The University of Chicago | |
| Drawn by | M. Bogdan | 5640 S. Ellis Ave. Chicago, IL 60637 | |
| R/D CHK | | TITLE | Rx FPGA |
| DATE | 9/19/11 | Near Transition VME Ca | |
| TIME | 11:17 am | | |
| QA CHK | | REV | A |
| | | DRW | 2743 |
| | | Sheet 5 of 12 | |