



IN[31:0]

Rx: To local FPGA
Tx: to Front Module

Rx: From Front Module
Tx: From Local FPGA

Engineer	M. Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M. Bogdan	TITLE	Size c
R&D CHK		I/O Buffers	
DATE:	9/19/11	Rear Transition VME Card	
TIME:	2:00 pm	REV A	DRW. 2743
QA CHK		Sheet 7 of 12	