0_IN[28:0]
1_IN[28:0]
2_IN[28:0]
3_IN[28:0]
4_IN[28:0]
5_IN[28:0]
VME_Data[31:0]
VME_Addr[26:2]
HOLDtoTx[7:0]
Internal_AUX[17:0]
HOLDtoEDRO[5:0]
Link_PWRDWN
FREEZEin
FREEZEout
Tx[31:0]
VME_AUX[10:0]
vme_write_read
vme_as
vme_ds
dir_trans
transceivers_OE
USB
Interface
LED_1
LED_2
LED_3
0.9Vcc
3.0Vcc
2.5Vcc
1.1Vcc
1.5Vcc
Sheet 12
FPGA
POWER
SM7745HV-50.0M
SM7745DV-100.0M
clkin2
clkin4
clkin1n
clkin1
clkin3n
clkin3
master_clock0
TEMPDIODEn
TEMPDIODEp
GND+
GND*
NIO_PULLUP
PORSEL
RREF1
RREF2
RREF3
RREF4
GXB_GND*
GXB_GND_CLK
USB-Blaster
DCLK
CONF_DONE
NCONFIG
ALTERA_DATA0
ASDO
NCE
nCSO
GND
JTAG Connector
TCK
TDO
TMS
TDI
MSEL0
MSEL1
MSEL2
TRST
NSTATUS
NCONFIG
CONF_DONE
NCE
EPCS64
Engineer M.Bogdan
Drawn by M.Bogdan
The University of Chicago
5640 S. Ellis Ave
Chicago, IL 60637
R&D CHK
TITLE
Tx FPGA
Rear Transition VME Card
Size C
DATE: 9/19/11
TIME: 11:17 am
QA CHK
REV A
DRW. 2743
Sheet 8 of 12