Lines common for all 4 DRS4 chips

Independent lines for each DRS4 chip

To Block FPGA DRS_Control[20:0]

ADC_Control[3:0]

ADC_OUT[21:0]

PDWN
Common to all AD9222

BIDAC[3:0]

DAC[7:0]

Lines common for all 4 DRS4 chips

Comp_IO[5:0]

Comp_IO[11:6]

Comp_IO[17:12]

Comp_IO[23:18]

Comp_IO[23:0]

Ch8_Out[1:0]

B1_33
DRS4

B1_34
AD9222

Internal Reference Configuration

PIN 0 - Exposed Paddle

Exposed Pad

LP2985IM5-2.5 +2.5V

LP2985IM5-2.5 +2.5V

LP2985IM5-3.3 +3.3V

+1.8V
Voltage common for all 5 ADCs.
From Sheet 10.

Engineer	M.Bogdan	**The University of Chicago**	
Drawn by	M.Bogdan	5620 S. Ellis Ave. Chicago, IL 60637	
R&D CHK		TITLE	*16-Ch, GHz AC/DC ADC Module*
DATE:	8/15/2012		Sampling_ADC Blo
TIME:	11:00 am		
QA CHK		REV B	DRW. 2793 Sheet 2_1