Sheet 6

VME_P1(159:0)

VMEbus_P1
ReservedBus(7:0)
Data(15:0)
Address(23:1)
AM(5:0)
VME_P1(159:0)
BR(3:0)
BGIN(3:0)
BGOUT(3:0)
IRQ(7:1)
GA*(4:0)
VME_Controls(17:0)

15:0
23:1
P1_AM(5:0)
noconn_BR(3:0)
noconn_IRQ(7:1)
P1_GA*(4:0)
VME_Controls(17:0)

A(31:1)

V1 SN74LVTH162245-3.3
V2 SN74LVTH162245-3.3
V8 SN74LVTH162245-3.3
V16 SN74LVTH162245-3.3
SOP

P1_SYSCLK
P1_DS1*
P1_LWORD*
P1_DS0*
P1_vme_write*
P1_IACK*
P1_IACKIN*
P1_AS*
P1_SYSFAIL*
P1_BERR
P1_DTACK

VME_P0(94:0)

P2_CUSTOM
Data(31:16)
Address(31:24)
VME_P2(159:0)
Trig_Ctrl(50:0)
Sheet 7

VME_P2(159:0)

31:16
31:24

D(31:0)

V18 SN74ABTE16245
V17 SN74LVTH162245-3.3
V19 SN74LVTH162245-3.3
V20 SN74ABTE16245
1DIR
2DIR
_OE
VCCBIAS

VME_etc(30:0)
_GA0
_GA1
_GA2
_GA3
_GA4
_IACKOUT
SYSCLK
_DS1
_LWORD
_DS0
_vme_write
_IACK
_IACKIN
_BERRIN
AM0
AM1
AM2
AM3
AM4
AM5
_DTACK
_AS
_BERR

_AS
_BERR
_DTACK
V12 SN74BCT760 DIP NULL
V14 390
V15 390
+3.3V

SISFAILIN_
V3 74VHC123
V4 10K
V5 0.1uF
V6 10K
V7 0.1uF
V9 NC7SZ125
V10 10K
V21 10K
SYSFAILOUT_
to_nConfig
V11 0
V13 0
Reconfig(1:0)

VME_Addr(31:2)
VME_OE
VME_DIR_TRANS
Local_VME_Data(31:0)

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Drawn by M.Bogdan			
R&D CHK	TITLE	Size C	
DATE: 9/19/12	*16-Ch, GHz AC/DC ADC Module* VME Interface		
TIME: 2:00 pm			
QA CHK	REV A	DRW. 2793	Sheet 5