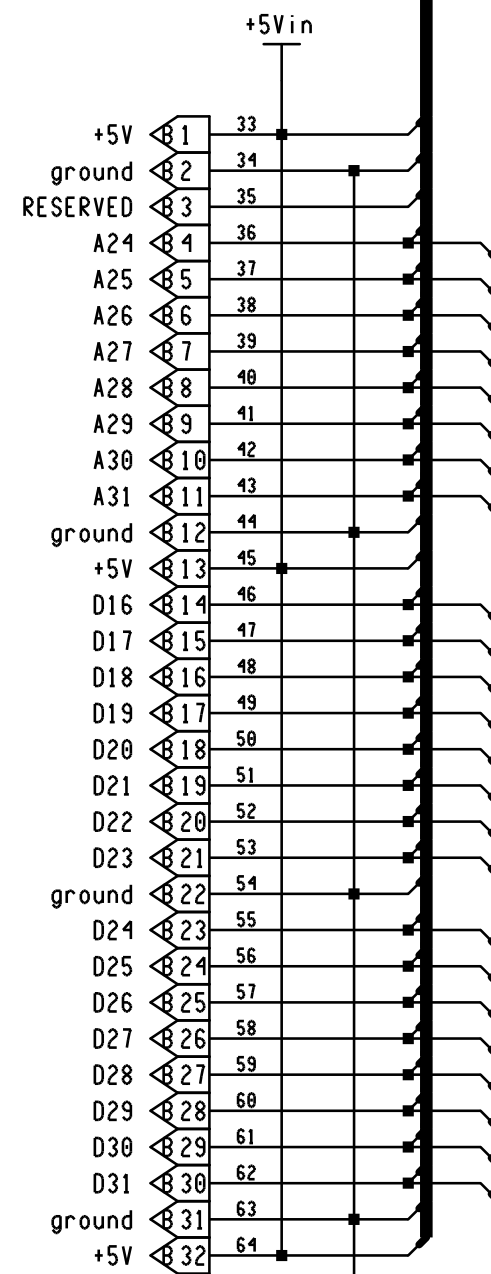
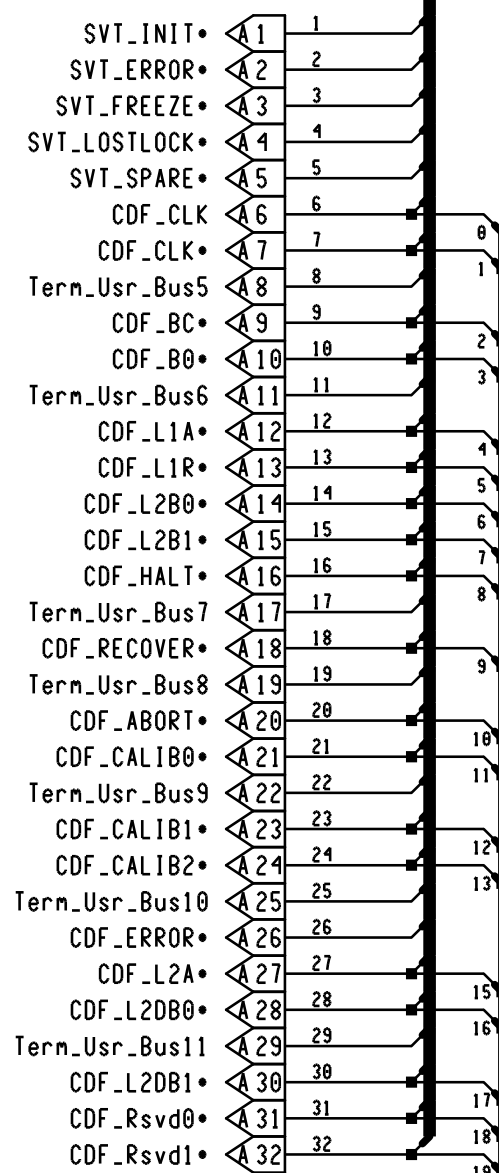
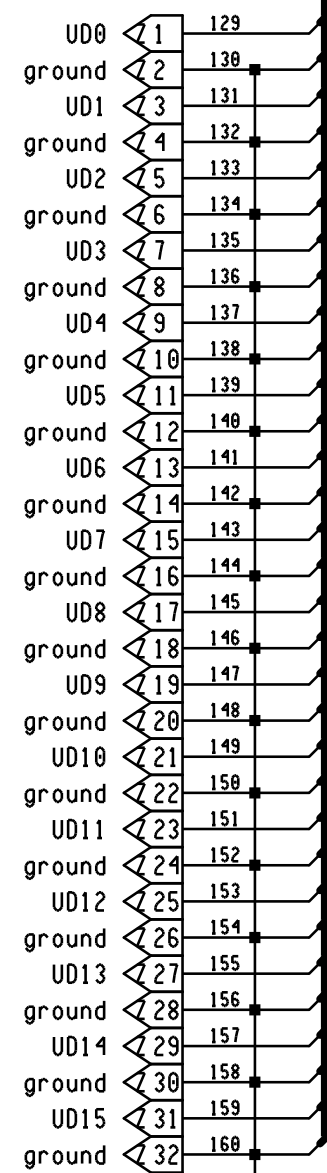
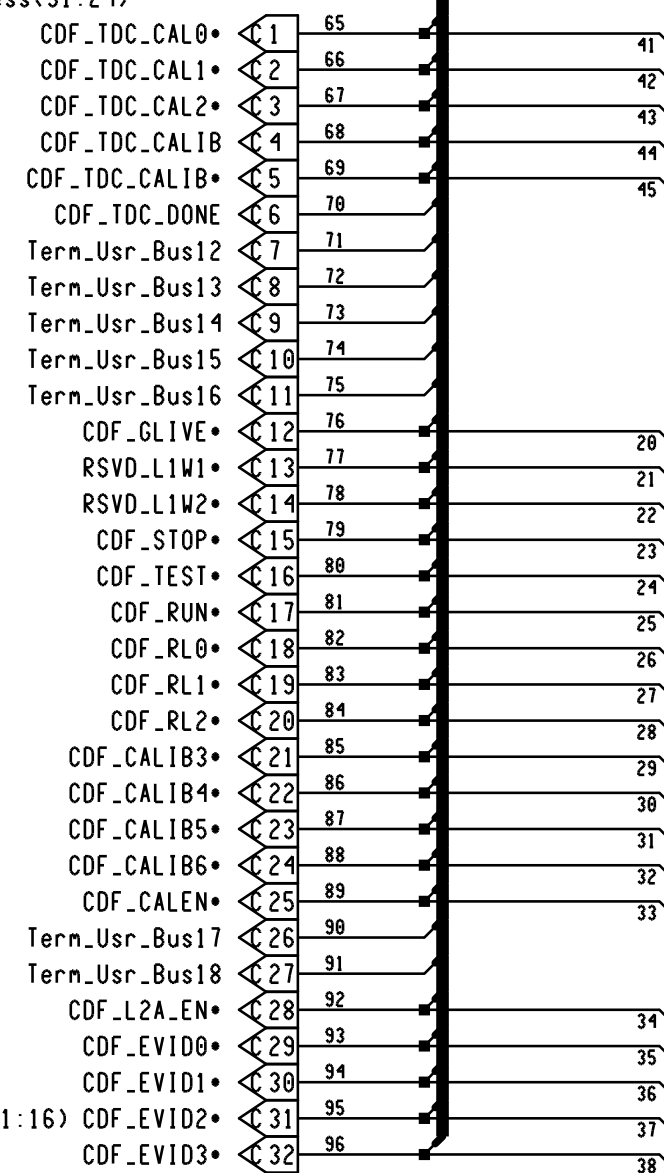


P2

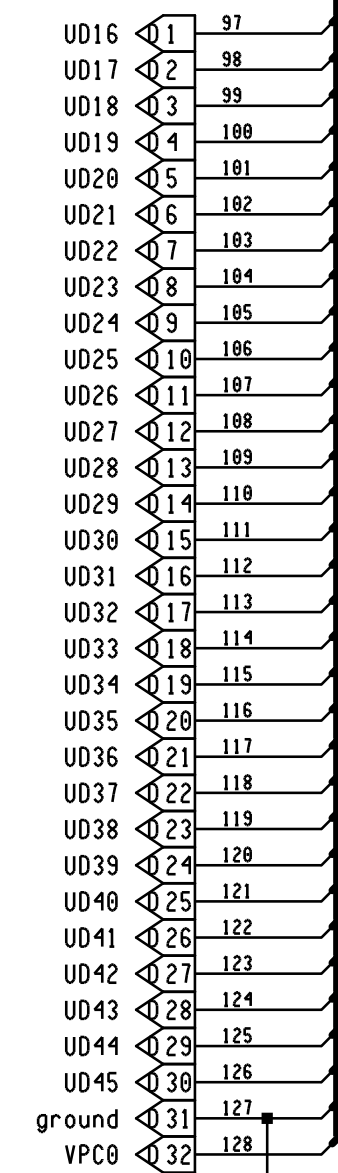
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Address(31:24)



Data(31:16)



Trig\_Ctrl(50:0)

Engineer	M. Bogdan	The University of Chicago 5620 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M. Bogdan		
R&D CHK		TITLE	Size B
DATE:	8/15/2012	16-Ch, GHz AC/DC ADC Module VME-P2	
TIME:	2:00 pm	REV	DRW. 2793
QA CHK		A	Sheet 7