

HTT Processor and Mezzanines Cooling


Mircea Bogdan
7/26/2018

The University of Chicago

ATCA Blade



EPE - Mezzanine FPGA - Power



[Visit the Online Power Management Resource Center](#)

Early Power Estimator
Stratix® 10
 Version 18.0.1, Build 07.05

Input Parameters		Thermal Power (W)	
Family	Stratix 10	Logic	18.265
Device	1SM21BH	RAM	14.161
Device Grade	Extended -3 Smart-VID	DSP	7.512
Package	F53	Clock	0.016
Transceiver Grade	HN3	PLL	0.392
Power Characteristics	Maximum	I/O	0.947
V _{CC} Voltage (mV)	VID	XCVR	5.926
Power Model Status	PRELIMINARY	HPS	0.000
		HBM	21.173
		P_{STATIC}	25.961
		Total Power Before SmartVID Savings	94.668
		SmartVID Power Savings	-3.607
		TOTAL (W)	91.060

Thermal Analysis Summary	
Junction Temp Mode	Detailed Thermal Model
User-Entered Junction Temp, T _J (°C)	
Ambient Temp, T _A (°C)	35
Max. Junction Temp, T _{J-MAX} (°C)	80
Recommended Ψ_{CA} (°C/W)	0.331
Max. Ψ_{JC} (°C/W)	0.163
Case Temperature T _{CASE} (°C)	65
Thermal Analysis Details	

[Intel recommends using Intel® Enpirion® Power Solutions with Intel® FPGAs](#)

Mircea Bogdan

Please, Download and Test!

Errors (0)

Calculation Mode	Solve for Maximum Tj
Apply Recommended Margin	No

Family	Stratix 10
Device	1SM21BH
Device Grade	Extended -3 Smart-VID
Package	F53
Transceiver Grade	HN3
Compact Model Name	1SM21BH_N_F53

Ambient Temp, T _A (°C)	25
Max. Junction Temp, T _{J-MAX} (°C)	80

The following values assume T_J=T_{J-MAX} for at least one of the dies in the package.
 Note that other dies in the package are typically below T_{J-MAX}.

Recommended Ψ_{CA} (°C/W)	0.441
Max. Ψ_{JC} (°C/W)	0.163
Case Temperature T _{CASE} (°C)	65

FPGA Core Power (W)	70.18
---------------------	-------

Transceiver Thermal Power (W)	
HSSI_2_1	0.00
HSSI_1_1	0.00
HSSI_0_1	0.00

HBM Thermal Power (W)	
HBM TOP_0	6.30
HBM BOT_0	6.30

FPGA Core Ψ_{JC} (°C/W)	0.106
------------------------------	-------

Transceiver Die Ψ_{JC} (°C/W)	
HSSI_2_1	0.000
HSSI_1_1	0.000
HSSI_0_1	0.000

HBM Die Ψ_{JC} (°C/W)	
HBM TOP_0	0.163
HBM BOT_0	0.161

FPGA Core TSD Offset (°C)	0
---------------------------	---

Transceiver Die TSD Offset (°C)	
HSSI_2_1	0
HSSI_1_1	0
HSSI_0_1	0

HSSI_2_0	6.55
HSSI_1_0	0.00
HSSI_0_0	1.73

HSSI_2_0	0.047
HSSI_1_0	0.000
HSSI_0_0	-0.036

HSSI_2_0	4
HSSI_1_0	0
HSSI_0_0	0

EPE - Mezzanine FPGA - Bottom

Total Power ~ 91W

80% Logic, 500MHz, HBM, etc.

http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_1.xls

Max Junction Temp ~ 80C

Max Case Temp ~ 65C

Air ~ 25C

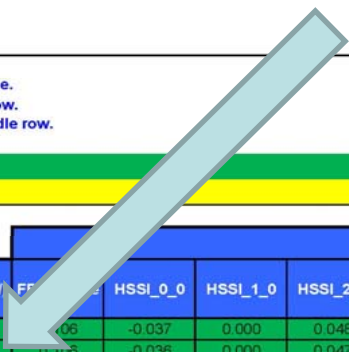
Heat Sink ~ 0.44C/W

Parameter variation with FPGA core junction temperature. Three values are provided for each parameter. The middle row contains FPGA core temperature and other parameters assuming the recommended Ψ_{CA} value above. The top row provides values of all parameters when FPGA core temperature is 5 degrees lower than in the middle row. The bottom row provides values of all parameters when FPGA core temperature is 5 degrees higher than in the middle row. The rows are color-coded, as follows:

Acceptable cooling solutions - all junction temperatures are at or below Max. Junction Temp, T_{J-MAX}.

Unacceptable cooling solutions - one or more junction temperatures are above Max. Junction Temp, T_{J-MAX}.

FPGA Core Junction Temperature (°C)	FPGA Core Power (W)	Overall Total Power (W)	Case Temperature T _{CASE} (°C)	Max. Junction Temperature (°C)	Ψ_{CA} (°C/W)	FPGA Core Ψ_{JC} (°C/W)	HSSI_0_0	HSSI_1_0	HSSI_2_0	HSSI_0_1	HSSI_1_1	HSSI_2_1	HBM TOP_0	HBM BOT_0
70	68.31	88.96	60	75	0.398	0.106	-0.05	-0.037	0.000	0.046	0.000	0.000	0.168	0.167
75	70.18	91.05	65	80	0.441	0.106	-0.036	0.000	0.047	0.000	0.000	0.000	0.163	0.161
80	72.26	93.37	70	85	0.480	0.106	-0.035	0.000	0.046	0.000	0.000	0.000	0.157	0.155



Thermal Return to Main

Errors (0)

Calculation Mode: **Solve for Maximum Tj**
 Apply Recommended Margin: **No**

Family	Stratix 10
Device	1SM21BH
Device Grade	Extended -3 Smart-VID
Package	F53
Transceiver Grade	HN3
Compact Model Name	1SM21BH_N_F53

Ambient Temp, T_A (°C): **35**
 Max. Junction Temp, $T_{j,MAX}$ (°C): **80**

The following values assume $T_j=T_{j,MAX}$ for at least one of the dies in the package.
 Note that other dies in the package are typically below $T_{j,MAX}$.

Recommended Ψ_{CA} (°C/W): 0.331
 Max. Ψ_{jc} (°C/W): 0.163
 Case Temperature T_{CASE} (°C): 65

FPGA Core Power (W): 70.19

Transceiver Thermal Power (W)	
HSSI_2_1	0.00
HSSI_1_1	0.00
HSSI_0_1	0.00

HBM Thermal Power (W)	
HBM TOP_0	6.30
HBM BOT_0	6.30

FPGA Core Ψ_{jc} (°C/W): 0.106

Transceiver Die Ψ_{jc} (°C/W)	
HSSI_2_1	0.000
HSSI_1_1	0.000
HSSI_0_1	0.000

HBM Die Ψ_{jc} (°C/W)	
HBM TOP_0	0.163
HBM BOT_0	0.161

FPGA Core TSD Offset (°C): 0

Transceiver Die TSD Offset (°C)	
HSSI_2_1	0
HSSI_1_1	0
HSSI_0_1	0

EPE - Mezzanine FPGA - Top

Total Power ~ 91W

80% Logic, 500MHz, HBM, etc.

http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_1.xls

Max Junction Temp ~ 80C

Max Case Temp ~ 65C

Air ~ 35C (Not yet Confirmed)

Heat Sink ~ 0.33C/W

HSSI_2_0	6.55
HSSI_1_0	0.00
HSSI_0_0	1.73

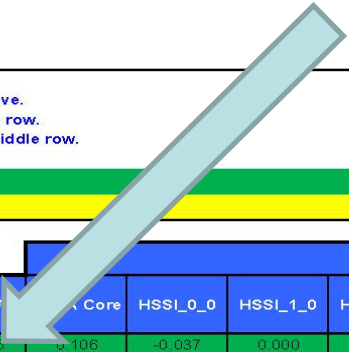
HSSI_2_0	0.047
HSSI_1_0	0.000
HSSI_0_0	-0.036

HSSI_2_0	4
HSSI_1_0	0
HSSI_0_0	0

Parameter variation with FPGA core junction temperature. Three values are provided for each parameter. The middle row contains FPGA core temperature and other parameters assuming the recommended Ψ_{CA} value above. The top row provides values of all parameters when FPGA core temperature is 5 degrees lower than in the middle row. The bottom row provides values of all parameters when FPGA core temperature is 5 degrees higher than in the middle row. The rows are color-coded, as follows:

Acceptable cooling solutions - all junction temperatures are at or below Max. Junction Temp, $T_{j,MAX}$
 Unacceptable cooling solutions - one or more junction temperatures are above Max. Junction Temp, $T_{j,MAX}$.

FPGA Core Junction Temperature (°C)	FPGA Core Power (W)	Overall Total Power (W)	Case Temperature T_{CASE} (°C)	Max. Junction Temperature (°C)	Ψ_{CA} (°C/W)	Ψ_{jc} (°C/W)								
						FPGA Core	HSSI_0_0	HSSI_1_0	HSSI_2_0	HSSI_0_1	HSSI_1_1	HSSI_2_1	HBM TOP_0	HBM BOT_0
70	68.32	88.97	60	75	0.295	0.106	-0.037	0.000	0.048	0.000	0.000	0.000	0.168	0.167
75	70.19	91.06	65	80	0.331	0.106	-0.036	0.000	0.047	0.000	0.000	0.000	0.163	0.161
80	72.26	93.38	70	85	0.373	0.106	-0.035	0.000	0.046	0.000	0.000	0.000	0.157	0.155



MODERATE CONFIGURATION | COPPER

SPECIFICATIONS

Overview

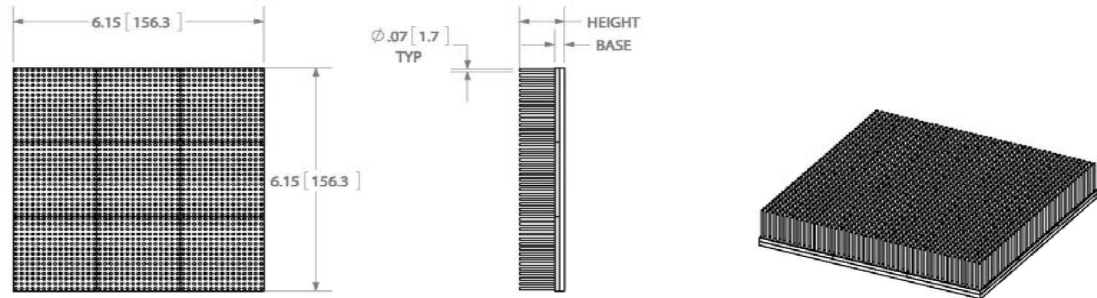
- Provides outstanding cooling power
- Rapid heat spreading
- Composed of nine forged heat sinks that are brazed on a copper base
- Recommended airspeed range: 400 to 1,000 LFM (2 to 5 m/s)
- RoHS compliant

Technical

- Material: Pure Copper
- Mfg. process: Cold forging
- Plating options: Electroless nickel, black zinc
- Base finish: Lapped
Flatness: Better than 0.001 in/in
Surface roughness: 16 RMS

Flexible Parameters

- Footprint (length and width)
- Height (pin length & base thickness)
- Single or multiple pins can be eliminated
- Comprehensive machining (holes, threads, clearances, etc.)



THE PIN FIN APPROACH: Round pin formations produce outstanding cooling power

P/N	Height in(mm)	Base in(mm)	Weight lb(g)	Thermal Resistance in °C/W			
				200(1)*	400(2)	600(3)	800(4)
4-626203U	0.30(7.6)	0.16(3.9)	2.26(1024)	1.3	0.77	0.54	0.41
4-626204U	0.40(10.2)	0.17(4.4)	2.68(1217)	0.74	0.41	0.28	0.21
4-626205U	0.50(12.7)	0.17(4.4)	2.93(1330)	0.52	0.28	0.19	0.14
4-626206U	0.60(15.2)	0.20(5.2)	3.47(1576)	0.40	0.21	0.14	0.11
4-626207U	0.70(17.8)	0.20(5.2)	3.73(1690)	0.32	0.17	0.12	0.084
4-626208U	0.80(20.3)	0.20(5.2)	3.98(1804)	0.27	0.15	0.097	0.071
4-626209U	0.90(22.9)	0.24(6.0)	4.54(2059)	0.24	0.13	0.084	0.062
4-626210U	1.00(25.4)	0.24(6.0)	4.79(2172)	0.21	0.11	0.073	0.055
4-626211U	1.10(27.9)	0.24(6.0)	5.04(2286)	0.19	0.10	0.066	0.049
4-626212U	1.20(30.5)	0.24(6.0)	5.29(2400)	0.17	0.090	0.060	0.044

Disclaimer: www.coolinnovations.com

*Air Speed in LFM (m/s)

Heat Sink - 1

> \$200/piece
> 2Lb/piece

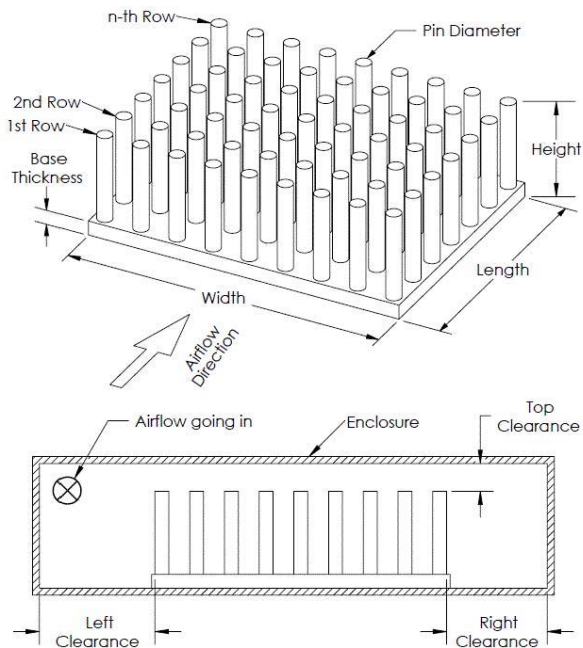
Needs Solid Mechanical Attachment

130x130x13mm Heat Sink ~1kg.

Heat Sink - 2

No Quote Yet

Example 1



Welcome to MyHeatSinks
Your source for cool solutions



Contact Us

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About & Contact

Advanced Round Pin Heat Sink Calculator

Your Input: Parameters Used in Calculation

Material: Copper (pure)	Pin Diameter: 1 mm	Width of Heat Source: 45.0 mm
Width: 150 mm	Number of Rows: 50	mm
Length: 150 mm	Pins Per Row: 50	Length of Heat Source: 45.0 mm
Height: 15 mm	Ambient Temperature: 47 °C	Top Clearance: 4.5 mm
Base Thickness: 3 mm	Heat to Dissipate: 90 W	Left Clearance: 1.0 mm
		Right Clearance: 1.0 mm

Calculation Result: Thermal Resistance, Pressure Drop & Base Temperature

Airflow Rate	Thermal Resistance	Pressure Drop	Base Temperature
0.5 m/s (~100 LFM)	0.30 °C/W	2.51 Pa (0.010 inH ₂ O)	74.4 °C
1.0 m/s (~200 LFM)	0.23 °C/W	7.50 Pa (0.030 inH ₂ O)	68.1 °C
1.5 m/s (~300 LFM)	0.21 °C/W	14.69 Pa (0.059 inH ₂ O)	65.5 °C
2.0 m/s (~400 LFM)	0.19 °C/W	24.01 Pa (0.096 inH ₂ O)	64.1 °C
2.5 m/s (~500 LFM)	0.18 °C/W	35.47 Pa (0.142 inH ₂ O)	63.1 °C
3.0 m/s (~600 LFM)	0.17 °C/W	49.04 Pa (0.197 inH ₂ O)	62.4 °C
3.5 m/s (~700 LFM)	0.16 °C/W	64.73 Pa (0.260 inH ₂ O)	61.8 °C
4.0 m/s (~800 LFM)	0.16 °C/W	82.54 Pa (0.331 inH ₂ O)	61.4 °C
4.5 m/s (~900 LFM)	0.16 °C/W	102.47 Pa (0.411 inH ₂ O)	61.0 °C
5.0 m/s (~1,000 LFM)	0.15 °C/W	124.51 Pa (0.500 inH ₂ O)	60.7 °C

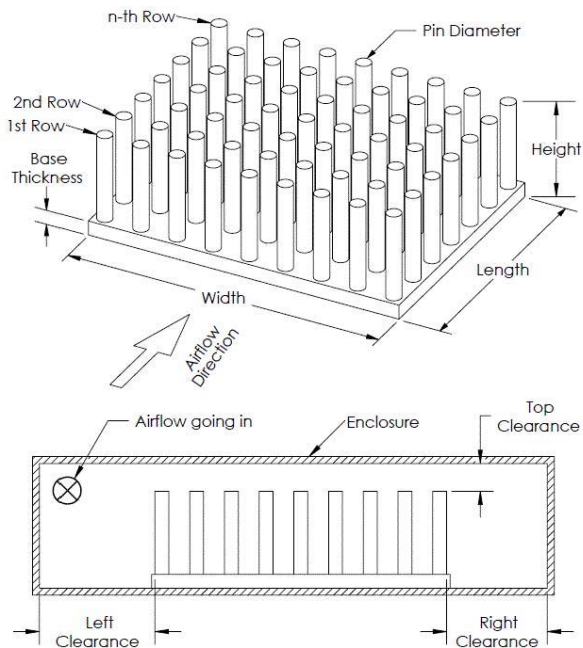
Please [click here to request a quote](#) for this heat sink.

The calculation result is for reference only. Customers are advised to build and test prototypes for all design projects.

Heat Sink - 2

No Quote Yet

Example 2



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Your source for cool solutions



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About & Contact

Advanced Round Pin Heat Sink Calculator

Your Input: Parameters Used in Calculation

Material: Copper (pure)	Pin Diameter: 1 mm	Width of Heat Source: 45.0 mm
Width: 130 mm	Number of Rows: 50	mm
Length: 130 mm	Pins Per Row: 50	Length of Heat Source:
Height: 15 mm	Ambient Temperature: 47 °C	45.0 mm
Base Thickness: 3 mm	Heat to Dissipate: 90 W	Top Clearance: 4.5 mm
		Left Clearance: 1.0 mm
		Right Clearance: 1.0 mm

Calculation Result: Thermal Resistance, Pressure Drop & Base Temperature

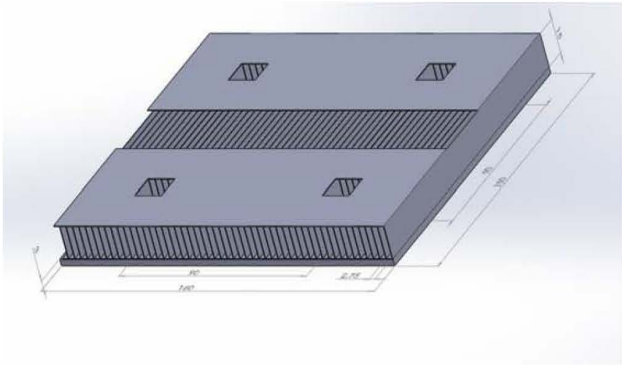
Airflow Rate	Thermal Resistance	Pressure Drop	Base Temperature
0.5 m/s (~100 LFM)	0.30 °C/W	2.59 Pa (0.010 inH ₂ O)	73.7 °C
1.0 m/s (~200 LFM)	0.22 °C/W	7.92 Pa (0.032 inH ₂ O)	66.7 °C
1.5 m/s (~300 LFM)	0.19 °C/W	15.60 Pa (0.063 inH ₂ O)	64.0 °C
2.0 m/s (~400 LFM)	0.17 °C/W	25.56 Pa (0.103 inH ₂ O)	62.5 °C
2.5 m/s (~500 LFM)	0.16 °C/W	37.75 Pa (0.152 inH ₂ O)	61.5 °C
3.0 m/s (~600 LFM)	0.15 °C/W	52.18 Pa (0.209 inH ₂ O)	60.8 °C
3.5 m/s (~700 LFM)	0.15 °C/W	68.83 Pa (0.276 inH ₂ O)	60.2 °C
4.0 m/s (~800 LFM)	0.14 °C/W	87.71 Pa (0.352 inH ₂ O)	59.8 °C
4.5 m/s (~900 LFM)	0.14 °C/W	108.81 Pa (0.437 inH ₂ O)	59.4 °C
5.0 m/s (~1,000 LFM)	0.13 °C/W	132.14 Pa (0.530 inH ₂ O)	59.1 °C

Please [click here to request a quote](#) for this heat sink.

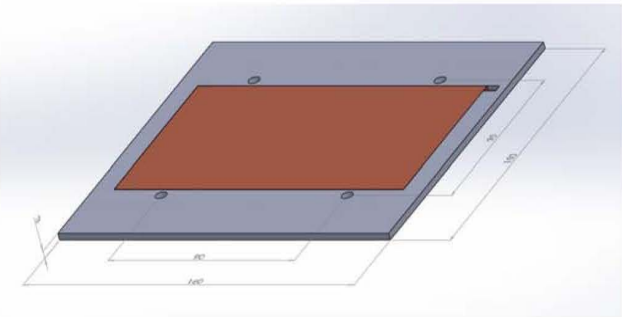
The calculation result is for reference only. Customers are advised to build and test prototypes for all design projects.

Heat Sink - 3

Forced Convection Fin Pack with Vapor Chamber Base



Module Dimension:W160*L150*H18mm
Base thickness:3mm
VC dimension: 82*145*3.0mm
Fin height:15mm
Fin Gap:2.75mm
Fin thickness:0.3mm



~\$335/piece + NRE (~\$6K)
~490g/piece

Heat Sink - 3

Simulation Received from Celsia Inc. Results for 11 - 15mm Fin Heights

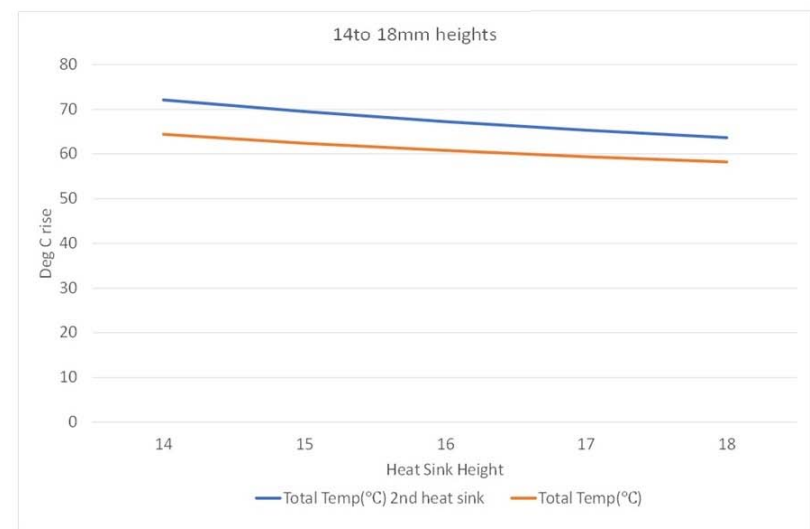
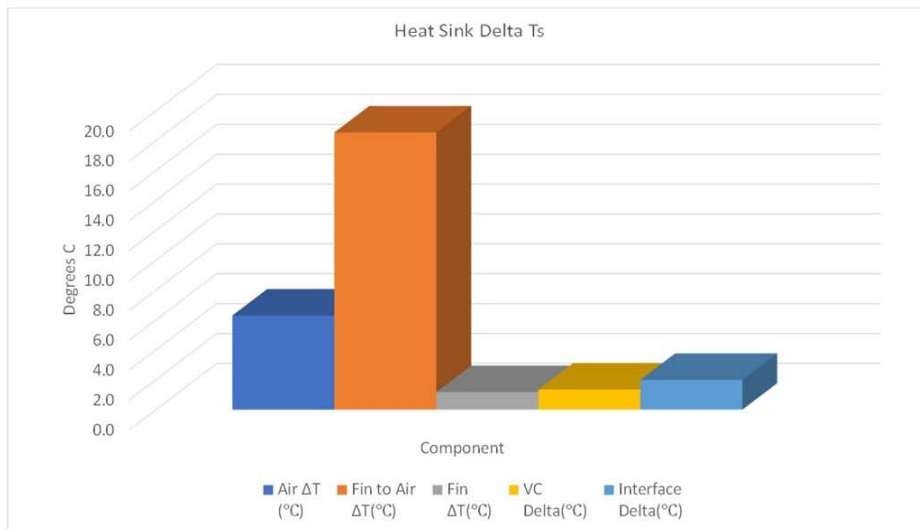
Series heat sinks

Q (W)	Source x	Source y	Source cm2	w/cm2	Ta (°C)	Finned W (mm)	Fin L (mm)	Fin H (mm)	Fin t (mm)	Base t Z (mm)	Total Height mm	Fin gap (mm)	CFM	Fin K (W/mk)	HPP	Fin's (pcs)	Fin area (ft²)	Air ΔT (°C)	Fin to Air ΔT(°C)	Fin ΔT(°C)	VC Delta(°C)	Interface Delta(°C)	HS Temp rise(°C)	Total Temp(°C)	Rth HS	Rth total
91	4.5	4.5	20	4.5	35	160	150	11	0.3	3	14	2.75	15	180	1	52	1.9	6.3	18.6	1.2	1.3	2	29	64	0.32	0.71
91	4.5	4.5	20	4.5	35	160	150	12	0.3	3	15	2.75	17	180	1	52	2.0	5.8	17.0	1.3	1.3	2	27	62	0.30	0.69
91	4.5	4.5	20	4.5	35	160	150	13	0.3	3	16	2.75	18	180	1	52	2.2	5.3	15.7	1.4	1.3	2	26	61	0.28	0.67
91	4.5	4.5	20	4.5	35	160	150	14	0.3	3	17	2.75	19	180	1	52	2.4	5.0	14.6	1.5	1.3	2	24	59	0.27	0.65
91	4.5	4.5	20	4.5	35	160	150	15	0.3	3	18	2.75	21	180	1	52	2.5	4.6	13.6	1.6	1.3	2	23	58	0.25	0.64

2nd heat sink

Q (W)	Source x	Source y	Source cm2	w/cm2	Ta (°C)	Finned W (mm)	Fin L (mm)	Fin H (mm)	Fin t (mm)	Base t Z (mm)	Total Height mm	Fin gap (mm)	CFM	Fin K (W/mk)	HPP	Fin's (pcs)	Fin area (ft²)	Air ΔT (°C)	Fin to Air ΔT(°C)	Fin ΔT(°C)	VC Delta(°C)	Interface Delta(°C)	HS Temp rise(°C)	Total Temp(°C)	Rth HS	Rth total
91	4.5	4.5	20	4.5	48	160	150	11	0.3	3	14	2	15	180	1	70	2.5	6.3	14.0	0.9	1.3	2	25	72	0.27	0.79
91	4.5	4.5	20	4.5	47	160	150	12	0.3	3	15	2	17	180	1	70	2.7	5.8	12.8	1.0	1.3	2	23	69	0.25	0.76
91	4.5	4.5	20	4.5	46	160	150	13	0.3	3	16	2	18	180	1	70	2.9	5.3	11.8	1.0	1.3	2	22	67	0.24	0.74
91	4.5	4.5	20	4.5	45	160	150	14	0.3	3	17	2	19	180	1	70	3.1	5.0	11.0	1.1	1.3	2	20	65	0.22	0.72
91	4.5	4.5	20	4.5	44	160	150	15	0.3	3	18	2	21	180	1	70	3.4	4.6	10.3	1.2	1.3	2	19	64	0.21	0.70

Total Temp(°C) 2nd heat sink



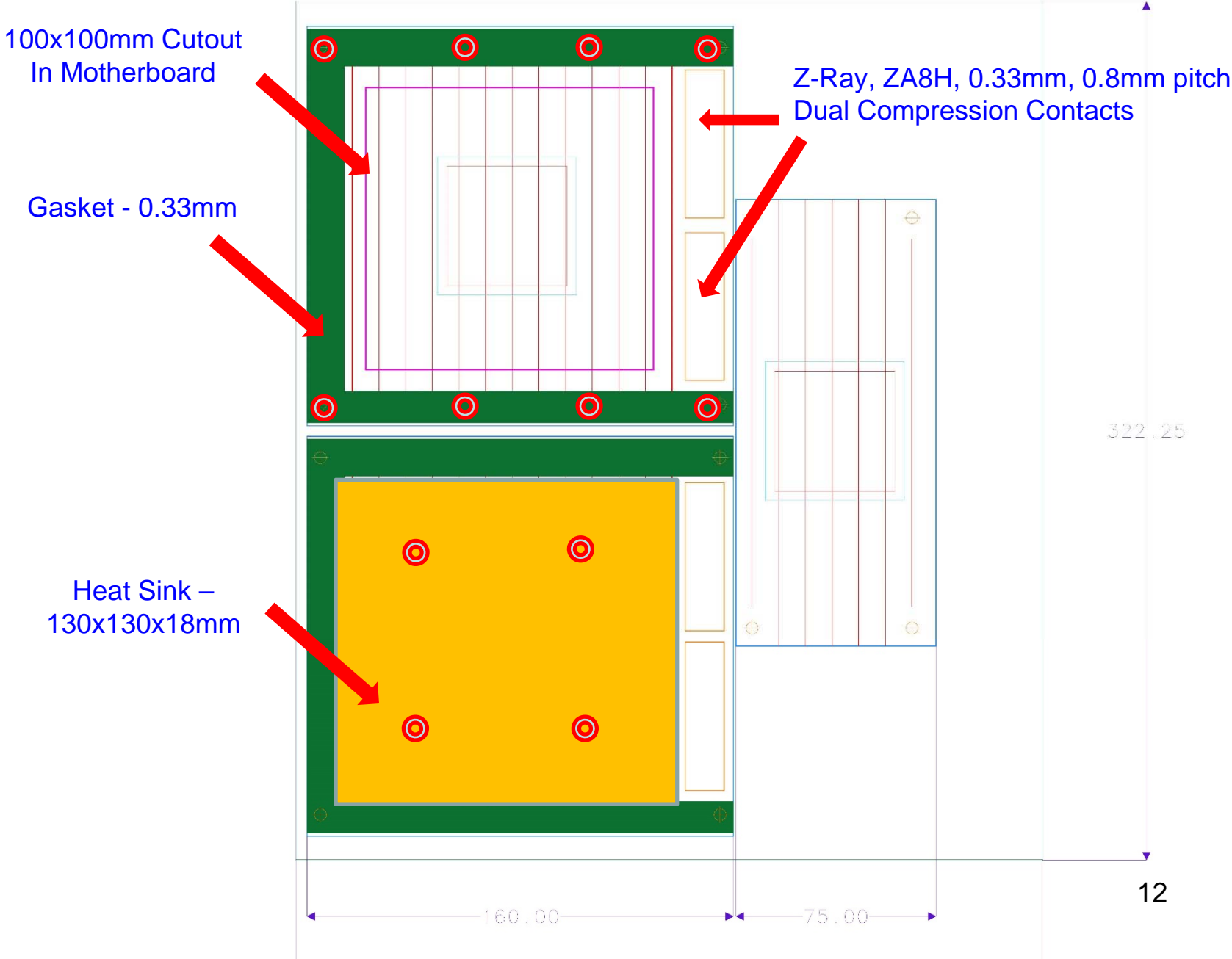
Comments – Questions -1

We have to reduce the gap between motherboards and mezzanines.

- Mezzanine Connectors Height < 0.5mm?
- Samtec Z-Ray Interposers?
- Can we cut hole in the mother board under each mezzanine card?
- Will mother board stay mechanically strong?
- Heavy Mezzanine Cards
 - Crate Manufacturer Discussion Needed?
 - We have to build and test dummy boards

Have to make sure the entire system is structurally sound before everything else

Mezzanine Mounting Example

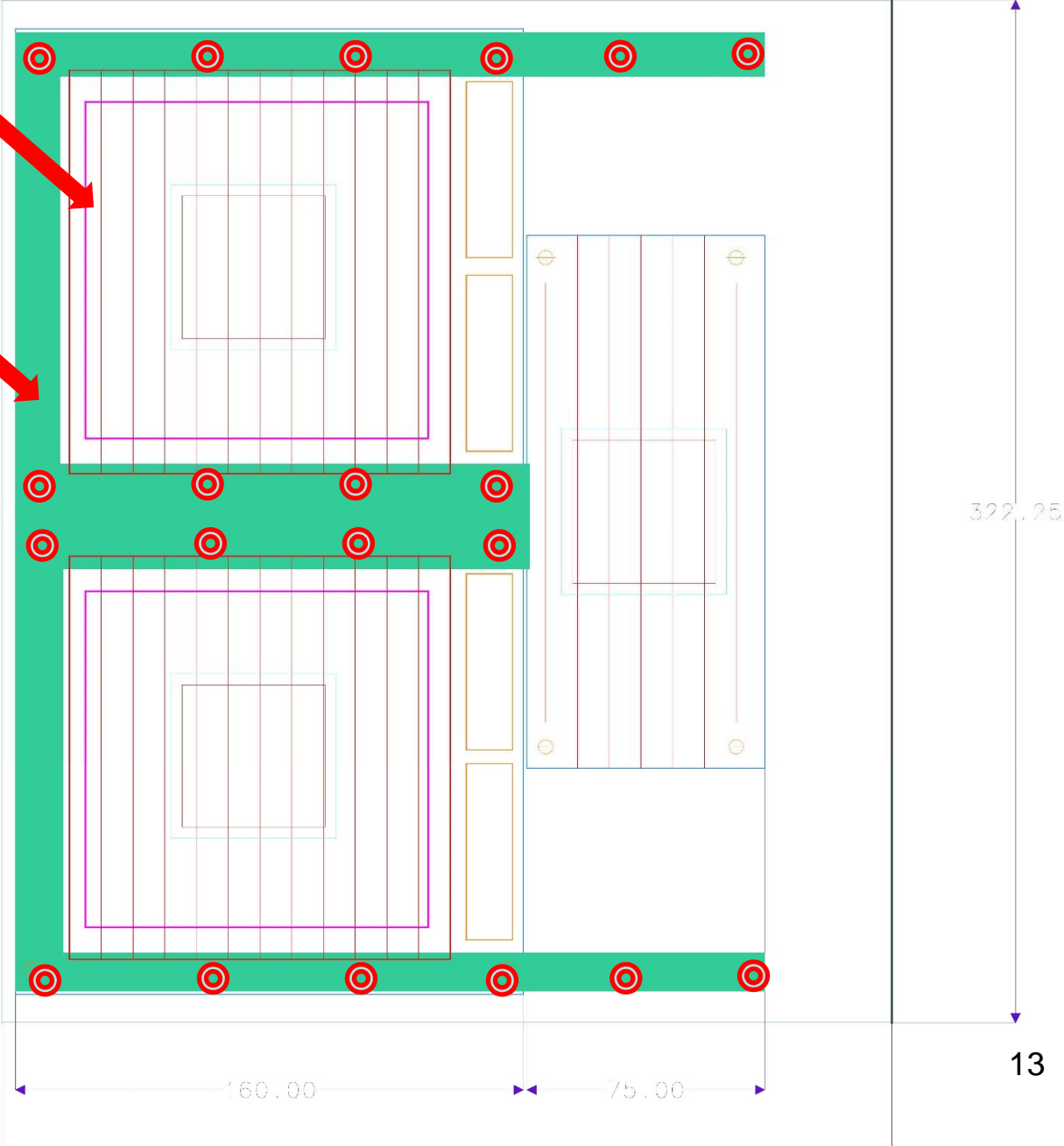


Mezzanine Mounting Example

100x100mm Cutout
In Motherboard

Stiffener – 1.5mm
On Bottom Side of
Motherboard

**May need Stiffener on
bottom of motherboard.**



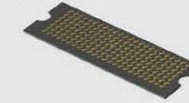
Z-Ray - ZA8H

Need to test this?

F-218



ZA8H-24-0.33-Z-07



ZA8H-06-0.33-Z-04



ZA8H-12-0.33-Z-07



(0.80 mm) .0315"

ZA8H SERIES

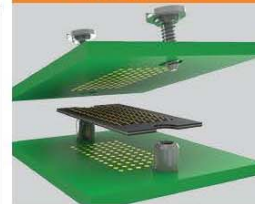
HIGH-SPEED DUAL COMPRESSION ARRAYS

SPECIFICATIONS

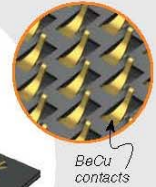
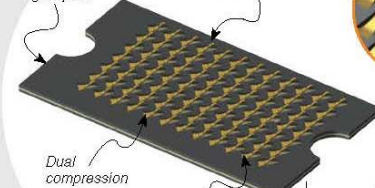
For complete specifications and recommended PCB layouts see www.samtec.com?ZA8H

Contact Material: BeCu
Plating: Au over 50 μm (1.27 μm) Ni
Core: Polyimide
Overlay: Polyimide
Current Rating: Testing Now!
Operating Temp Range: Testing Now!
RoHS Compliant: Yes

APPLICATION



Extreme low profile provides shortest signal path
 25 g normal force with (0.20 mm) .008" contact deflection



Dual compression

Up to 168 contacts

(0.33 mm) .013" height

HIGH-SPEED CHANNEL PERFORMANCE

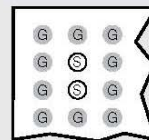
0.33 mm Stack Height

Rating based on Samtec reference channel. For full SI performance data visit Samtec.com or contact SIG@samtec.com

NRZ

56 Gbps

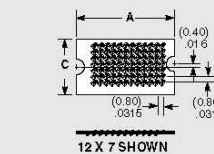
SIGNAL MAPPING



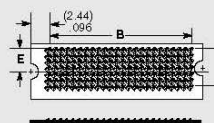
To meet 56 Gbps performance, footprint must meet specific signal/ground configurations. Contact the Signal Integrity Group at SIG@samtec.com for recommended signal routing.

ZA8H	NO. OF POSITIONS	HEIGHT	PLATING	ROWS
	-06, -12, -24 (See Chart Below For Number Of Pairs)	-0.33 = (0.33 mm) .013" Height	-Z = 6 μm (0.15 μm) Gold on contact over 40 μm to 100 μm (1.02 μm-2.54 μm) Nickel	-04 = Four Rows -07 = Seven Rows

ARRAY	PAIR COUNT
06 X 04	2
12 X 04	4
12 X 07	8
24 X 07	16



12 X 7 SHOWN



24 X 7 SHOWN

NO. OF POSITIONS	A	B
-06	(7.80) .307	(4.000) .1575
-12	(12.80) .496	(8.800) .3465
-24	(22.20) .874	(18.400) .7244

NO. OF ROWS	C	D	E
-04	(4.70) .185	(2.400) .0945	(1.75) .069
-07	(7.10) .280	(4.800) .1890	(2.95) .116

Note:
Some lengths, styles and options are non-standard, non-returnable.

Due to technical progress, all designs, specifications and components are subject to change without notice.

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All parts within this catalog are built to Samtec's specifications. Customer specific requirements must be approved by Samtec and identified in a Samtec customer-specific drawing to apply.

Comments – Questions -3

- Over 360W/slot - Not a Trivial Issue
- It looks like it can be done with sufficient power and cooling

Thermal Simulation in Steps:

- Simulate one and two mezzanines
 - In Chicago, we plan to download and test FloTERM in the next few weeks. We'll see how this goes.
- One full ATCA Blade and the Full Crate will need to be simulated in the future.
- Does vendor simulate the crates they manufacture?

Comments – Questions - 4

We have to agree about acceptable architecture: connectors, PCB geometries, PCB cutouts, etc. before we start simulating.

If we end up with not enough margin:

- Double width ATCA Carrier Blade?