HTT Mezzanines
Thermal Simulation

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The University of Chicago

Thermal	Return to Main

Errors (0)

Calculation Mode	Solve for Maximum Tj
Apply Recommended Margin	No

Ambient Temp, T_A (°C)	25
Max. Junction Temp, $T_{J\text{-}MAX}$ (°C)	80

Family	Stratix 10
Device	1SM21BH
Device Grade	Extended -3 Smart-VID
Package	F53
Transceiver Grade	HN3
Compact Model Name	1SM21BH_N_F53

The following values assume T_J=$T_{J\text{-}MAX}$ for at least one of the dies in the package.
Note that other dies in the package are typically below $T_{J\text{-}MAX}$.

Recommended Ψ_{CA} (°C/W)	0.441
Max. Ψ_{JC} (°C/W)	0.163
Case Temperature T_{CASE} (°C)	65

FPGA Core Power (W)	70.18

*

Transceiver Thermal Power (W)	
HSSI_2_1	0.00
HSSI_1_1	0.00
HSSI_0_1	0.00

HSSI_2_0	6.55
HSSI_1_0	0.00
HSSI_0_0	1.73

*

HBM Thermal Power (W)	
HBM TOP_0	6.30
HBM BOT_0	6.30

*

FPGA Core Ψ_{JC} (°C/W)	0.106

Transceiver Die Ψ_{JC} (°C/W)	
HSSI_2_1	0.000
HSSI_1_1	0.000
HSSI_0_1	0.000

HSSI_2_0	0.047
HSSI_1_0	0.000
HSSI_0_0	-0.036

HBM Die Ψ_{JC} (°C/W)	
HBM TOP_0	0.163
HBM BOT_0	0.161

FPGA Core TSD Offset (°C)	0

Transceiver Die TSD Offset (°C)	
HSSI_2_1	0
HSSI_1_1	0
HSSI_0_1	0

HSSI_2_0	4
HSSI_1_0	0
HSSI_0_0	0

EPE - Mezzanine FPGA - Bottom

Total Power ~ 91W

80% Logic, 500MHz, HBM, etc.

http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_1.xls

Max Junction Temp ~ 80C
Air ~ 25C

(*) Power applied to corresponding parts of thermal model. Intel supplied FloTHERM model includes thermal specs of various parts of Stratix10Mx chip.

Parameter variation with FPGA core junction temperature. Three values are provided for each parameter.
The middle row contains FPGA core temperature and other parameters assuming the recommended Ψ_{CA} value above.
The top row provides values of all parameters when FPGA core temperature is 5 degrees lower than in the middle row.
The bottom row provides values of all parameters when FPGA core temperature is 5 degrees higher than in the middle row.
The rows are color-coded, as follows:
Acceptable cooling solutions - all junction temperatures are at or below Max. Junction Temp, $T_{J\text{-}MAX}$.
Unacceptable cooling solutions - one or more junction temperatures are above Max. Junction Temp, $T_{J\text{-}MAX}$.

						Ψ_{JC} (°C/W)								
FPGA Core Junction Temperature (°C)	FPGA Core Power (W)	Overall Total Power (W)	Case Temperature T_{CASE} (°C)	Max. Junction Temperature (°C)	Ψ_{CA} (°C/W)	FPGA Core	HSSI_0_0	HSSI_1_0	HSSI_2_0	HSSI_0_1	HSSI_1_1	HSSI_2_1	HBM TOP_0	HBM BOT_0
70	68.31	88.96	60	75	0.398	0.106	-0.037	0.000	0.048	0.000	0.000	0.000	0.168	0.167
75	70.18	91.05	65	80	0.441	0.106	-0.036	0.000	0.047	0.000	0.000	0.000	0.163	0.161
80	72.26	93.37	70	85	0.480	0.106	-0.035	0.000	0.046	0.000	0.000	0.000	0.157	0.155

Temperature Simulation with FloTHERM - 1

Estimated FPGA Power with Intel Stratix EPE:

70.18 + 6.3 + 6.3 + 6.55 + 1.73 = 91.06 [W]

Created two different thermal models for the FPGA:

Generic 2-Resistor Model – 45x45x4mm cuboid, with 91W power concentrated in the middle plane, and 0.16C/W and 5C/W estimated thermal resistances to the top and bottom sides.

Detailed Model - All five EPE power estimates were added to an Intel FloTHERM Stratix 10Mx thermal model. This model has separate dies like the actual FPGA.

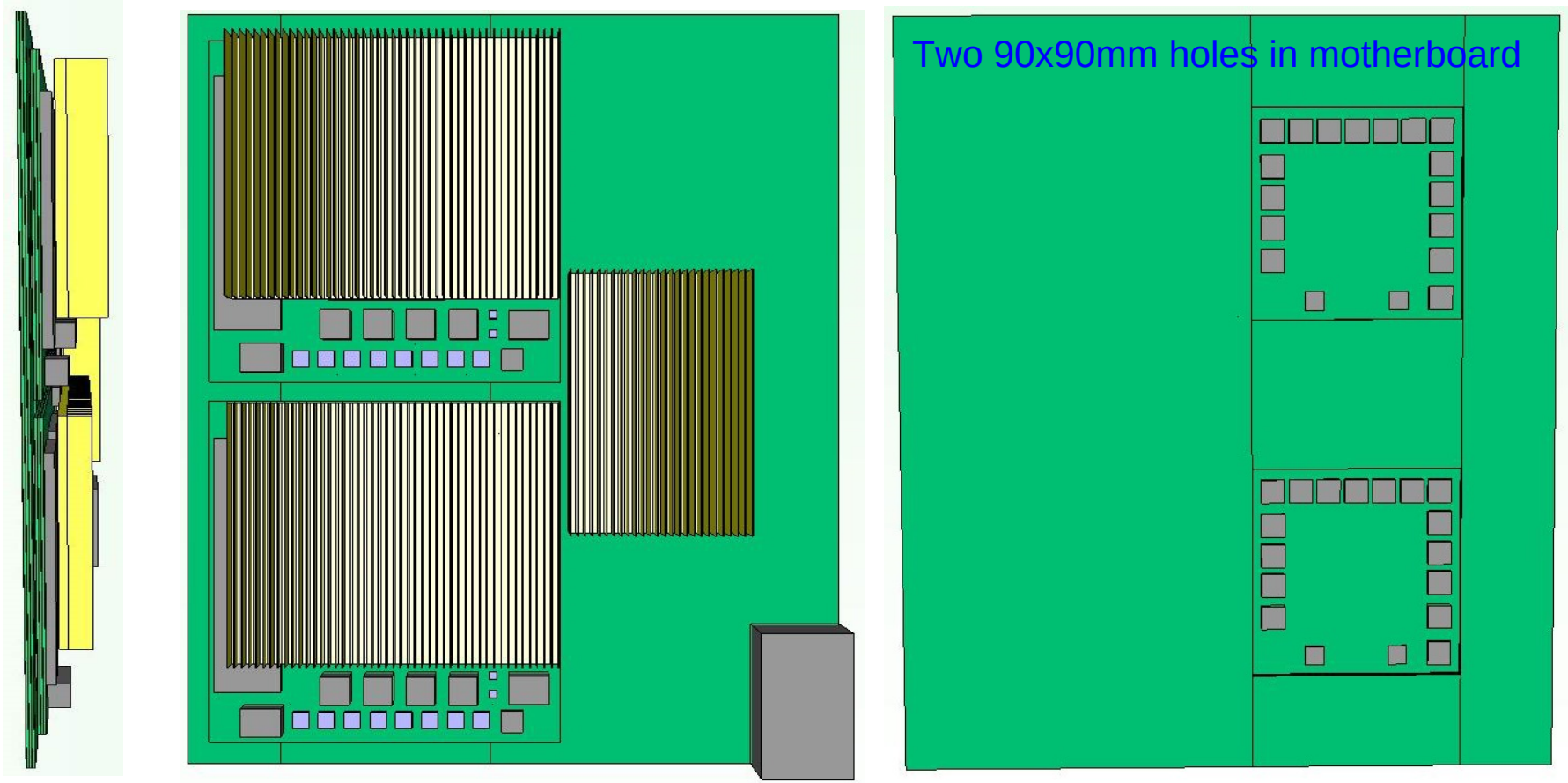
Temperature Simulation with FloTHERM - 2

- Build six mezzanine card thermal models:
  - 150x146mm with 0.5mm Connector (two 90x90mm holes in motherboard);
  - 150x146mm with 2mm Connector;
  - 74x300mm with 0.5mm Connector (one 140x150mm hole in motherboard);
  - 74x300mm with 2mm Connector;
  - 170x146mm with 0.5mm Connector (two 110x90mm holes in motherboard);
  - 170x146mm with 0.5mm Connector and 1mm taller Heatsinks

Each Mezzanine Card:

- FPGA-Heatsink; 38 ICs (24W), 48 caps 2917, 120 caps 1206.
- Temperature Monitor Points in each die and active component.
- Surface Temperatures for all parts is saved during simulation.

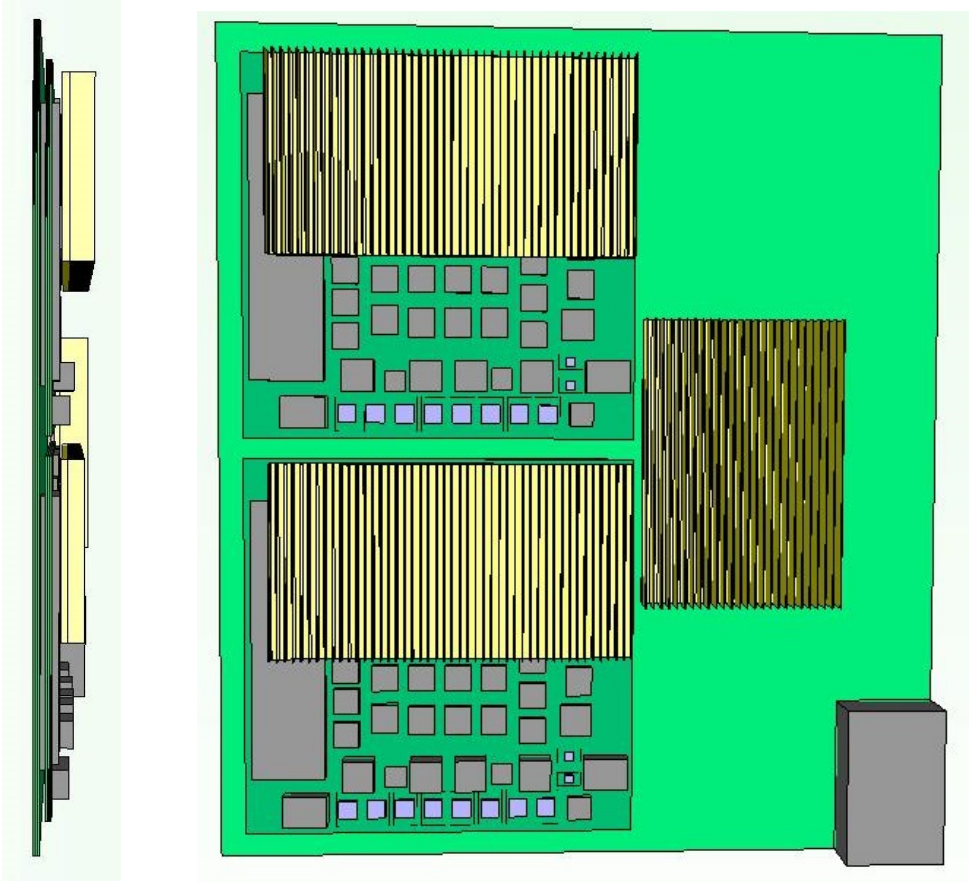
A - Square Mezzanines with 0.5mm Connectors:



- Two 150x146mm Mezzanine Cards with 0.5mm Connector
- Max. Height from Motherboard Top Side: 0.5+2.5+4+3.2+11.3=21.5mm
- Heatsink Sizes Optimized for min Temp at 4m/s (tested 100 Scenarios in FloTHERM)
  - Bottom Heatsink: Base = 138x110x2.7mm; 45 Fins = 0.3x110x7.3mm
  - Top Heatsink: Base = 138x110x3.2mm; 45 Fins = 0.3x110x11.3m

Mezzanine PCB Height=2.5mm, FPGA Height=4mm

B - Square Mezzanines with 2mm Connectors:

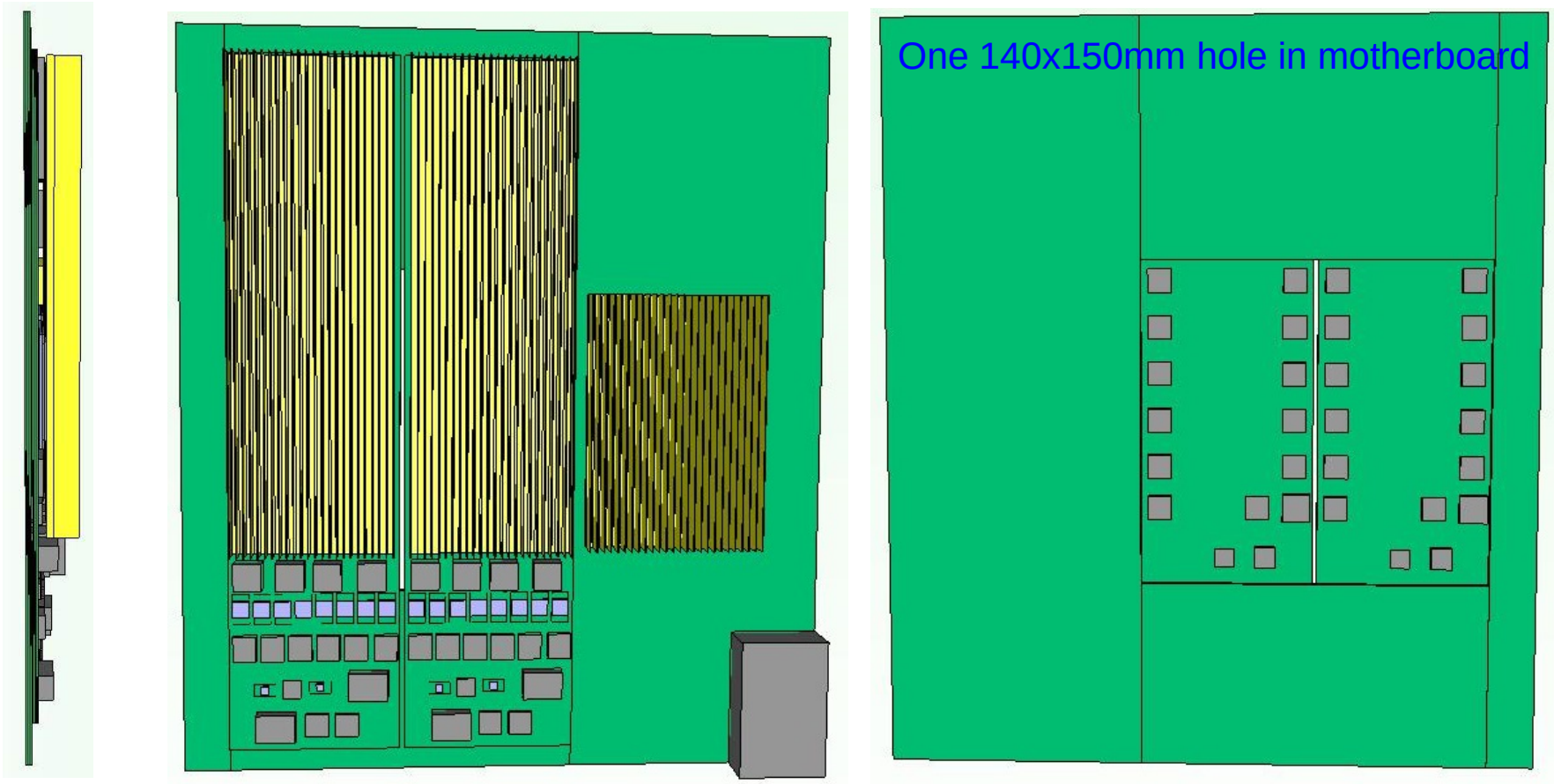


- No Holes in Motherboard
- All active components on Top of Mezzanine Card

- Two 150x146mm Mezzanine Cards with 2mm Connector
- Max. Height from Motherboard Top Side: 2+2.5+4+3.2+9.8=21.5mm
- Heatsink Sizes:
  - Bottom Heatsink: Base = 138x75x2.7mm; 45 Fins = 0.3x75x6.5mm
  - Top Heatsink: Base = 138x75x3.2mm; 45 Fins = 0.3x75x9.8mm

Mezzanine PCB Height=2.5mm, FPGA Height=4mm

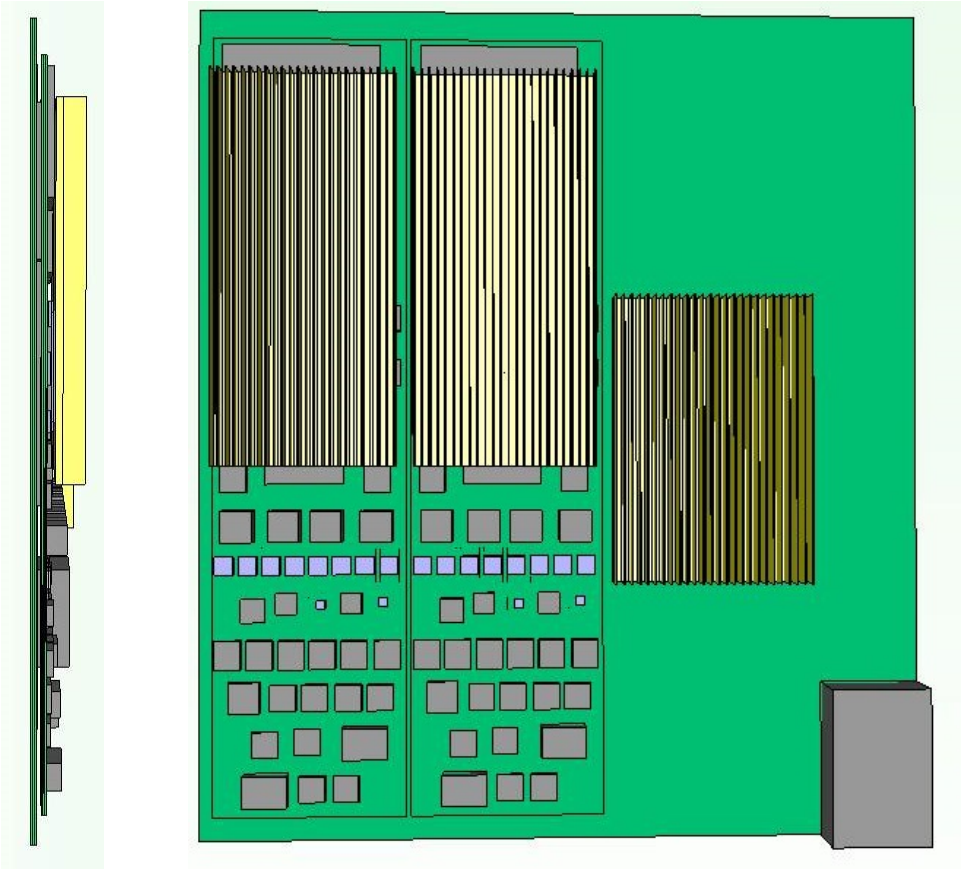
C - Long Mezzanines with 0.5mm Connectors:



- Two 74x300mm Mezzanine Cards with 0.5mm Connector
- Heatsinks Size: Base = 69x210x3.2mm; 24 Fins = 0.3x210x11.3mm
- Max. Height from Motherboard Top Side: 0.5+2.5+4+3.2+11.3=21.5mm

Mezzanine PCB Height=2.5mm, FPGA Height=4mm

D - Long Mezzanines with 2mm Connectors:



- No Holes in Motherboard
- All active components on Top of Mezzanine Card

- Two 74x300mm Mezzanine Cards with 2mm Connector
- Max. Height from Motherboard Top Side: 2+2.5+4+3.2+9.8=21.5mm.
- Heatsinks Size:
  - Base = 69x150x3.2mm; 24 Fins = 0.3x150x9.8mm

Mezzanine PCB Height=2.5mm, FPGA Height=4mm

Temperature Simulation with FloTHERM - 3

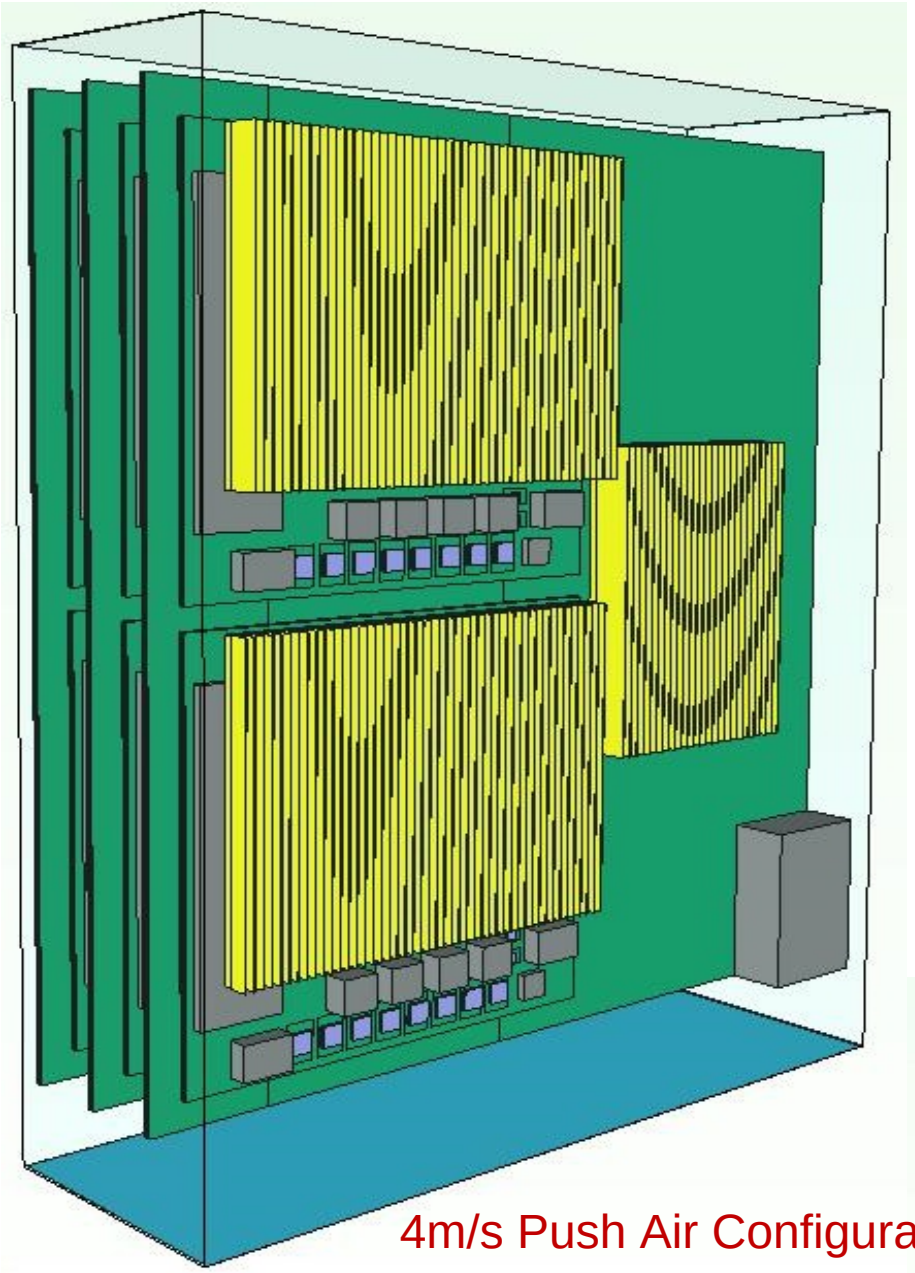
Created a 282x100x366mm Chassis Model that holds three 280x322mm ATCA Blades, spaced at 30.5mm intervals.

The four lateral sides of chassis are made of 1mm Aluminum

Depending on air flow method, the Top and Bottom sides are Fixed Flow Smart Parts (FFSP), or are open to the 25C Ambient.

Three Blades with Mezzanines of the same kind were placed in Chassis and this assembly was solved to 1C temperature accuracy, and stable temperatures at each Monitor Point.

This was repeated for each of the six types of mezzanine cards, for push, pull, and for push-pull air flow methods, and for different air speeds.



4m/s Push Air Configuration

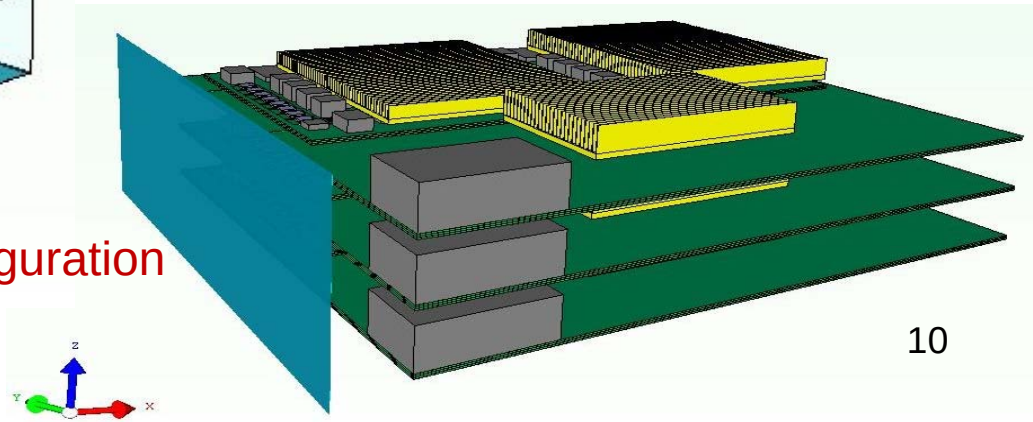
Chassis Model

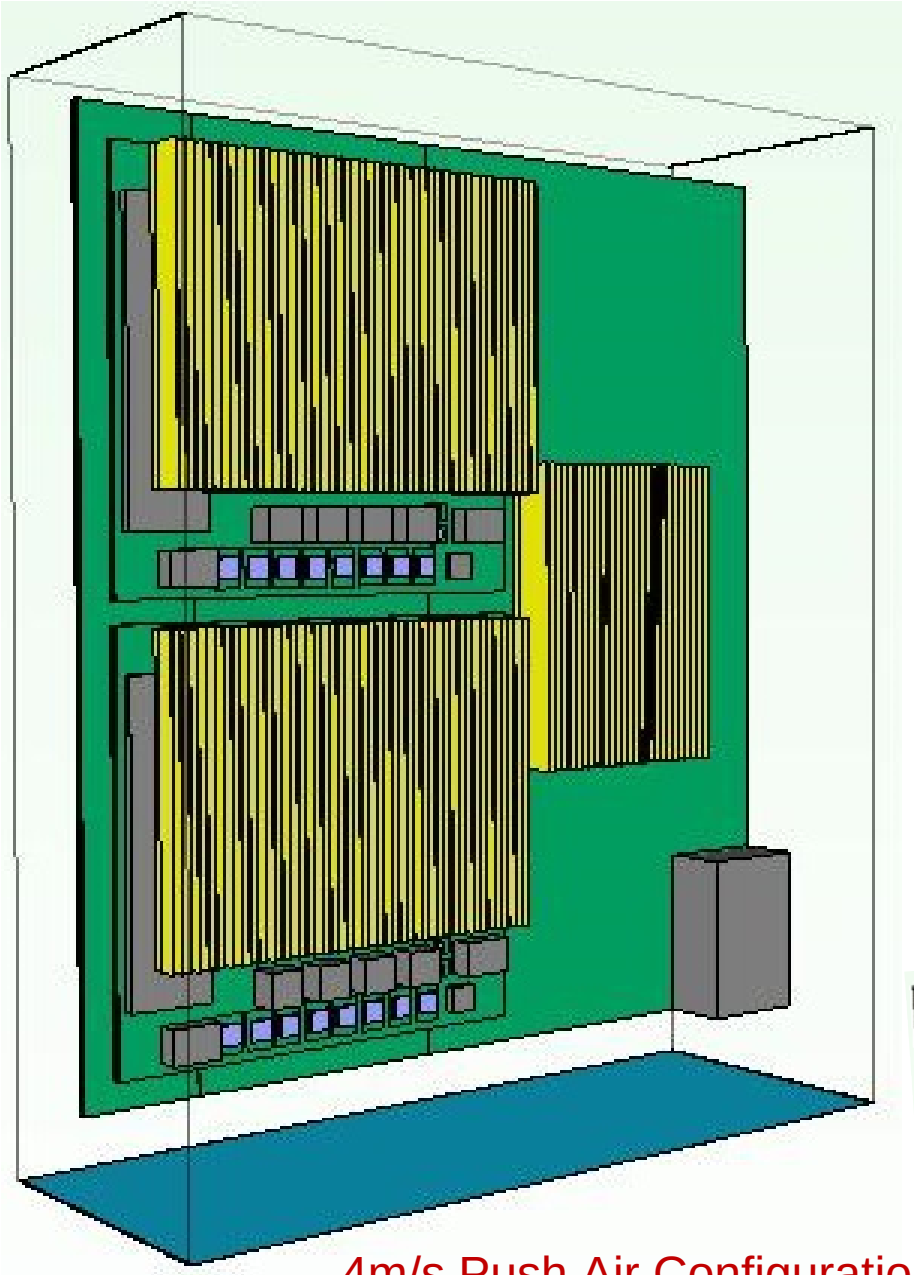
Three different air flow configurations were simulated:

- PUSH: FFSP at the bottom with top open
- PULL: bottom open and FFST on top
- PUSH-PULL: FFST on both bottom and top

Middle Blade between identical blades at 30.5mm best represents actual ATCA

~ 12 hours solve time for each simulation





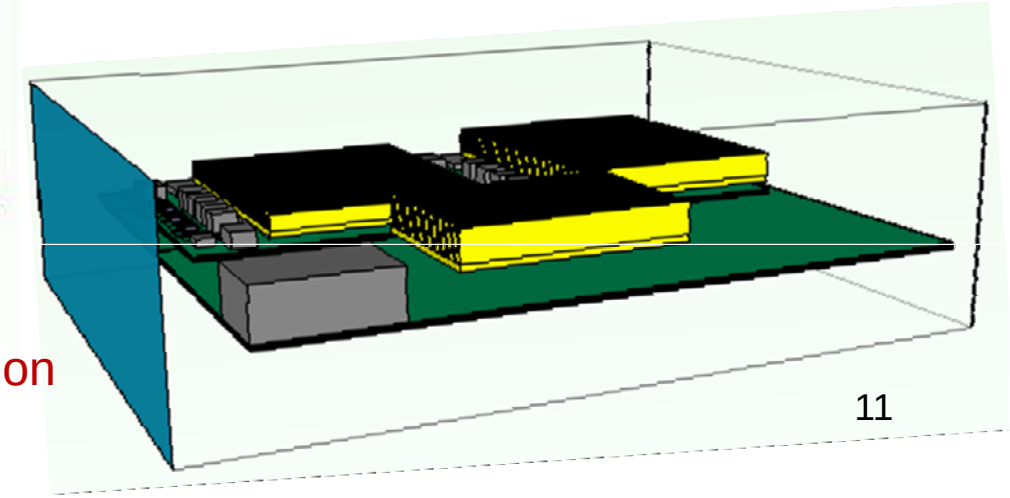
4m/s Push Air Configuration

Chassis Model Loaded with 1, 2 or 3 Blades

Simulating the same chassis with only one or two blades inside, gives different Max Junction Temperature Results:

- 74.13C with Blade_0, Blade_1, Blade_2
- 88.26C with only Blade_1
- 82.95C, 78.36C - only Blade_0, Blade_2
- 79.35C, 81.87C - only Blade_0, Blade_1

Removing blades from crate will cause substantial temperature increases, even if front plates are installed.

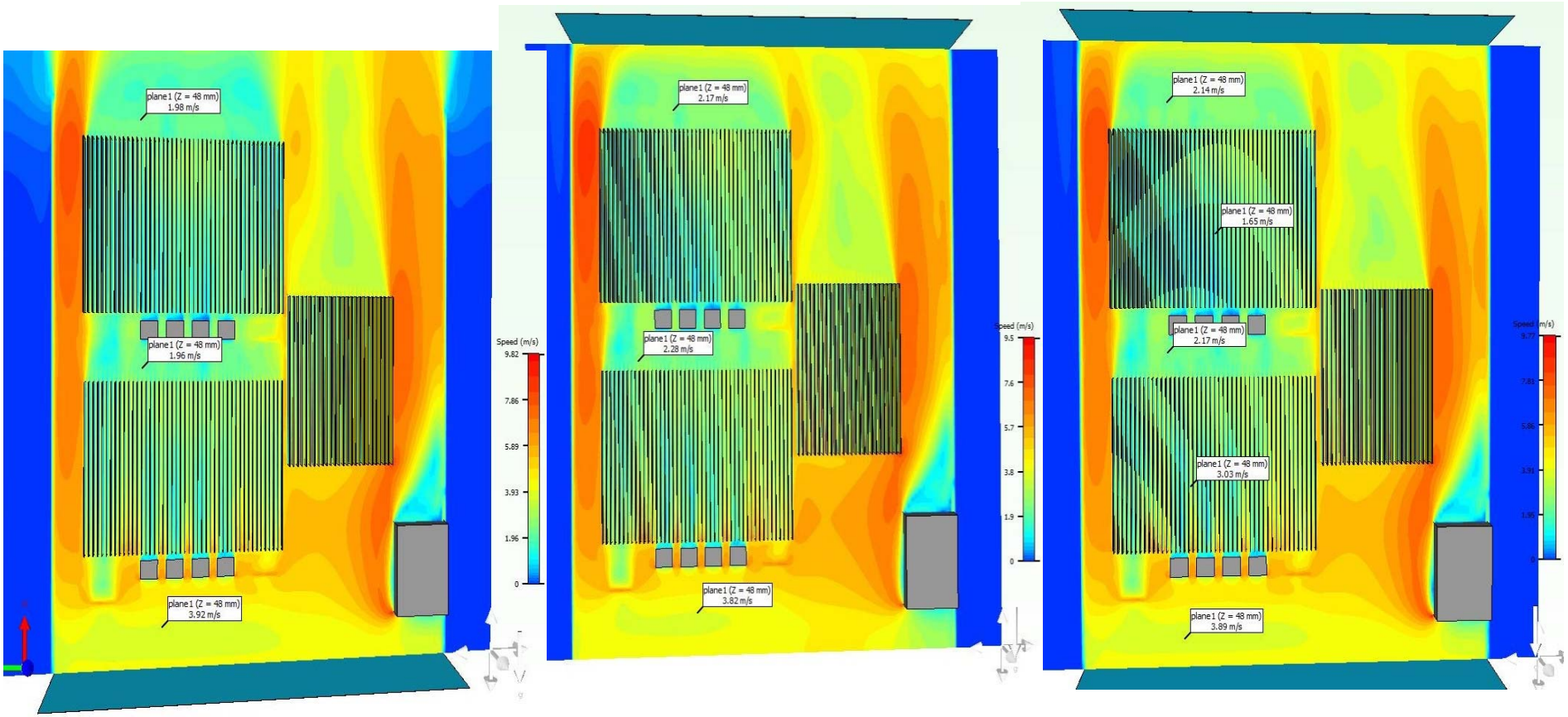


Local air speed at 8mm over middle motherboard for 3 FFSP configurations

4m/s Fixed Flow from Bottom In

4m/s Fixed Flow from Top Out

4m/s Fixed Flow from Bottom In and from Top Out



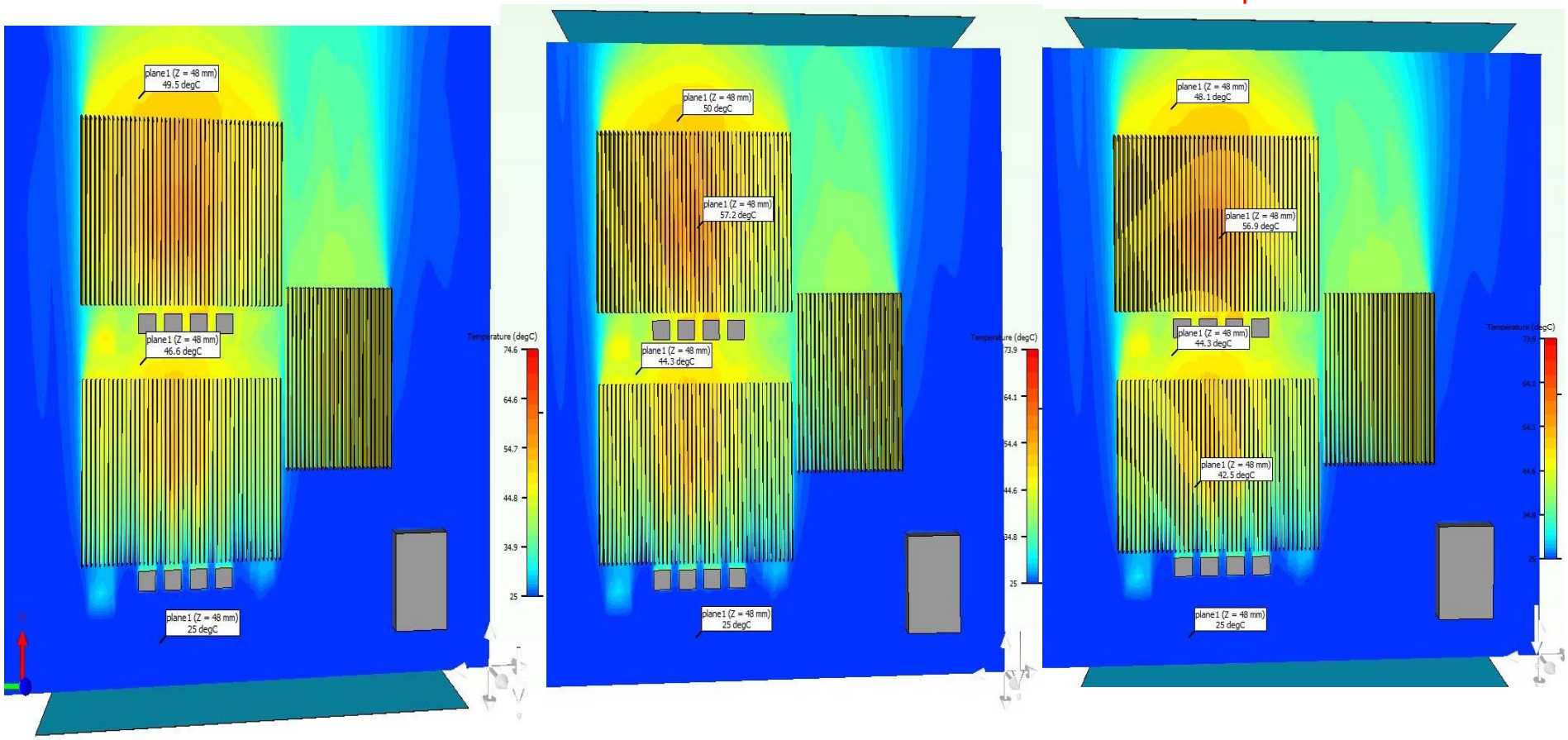
Very small local air speed variations for the same FFSP air speed.

Local air temps at 8mm over middle motherboard for 3 FFSP configurations

4m/s Fixed Flow from Bottom In

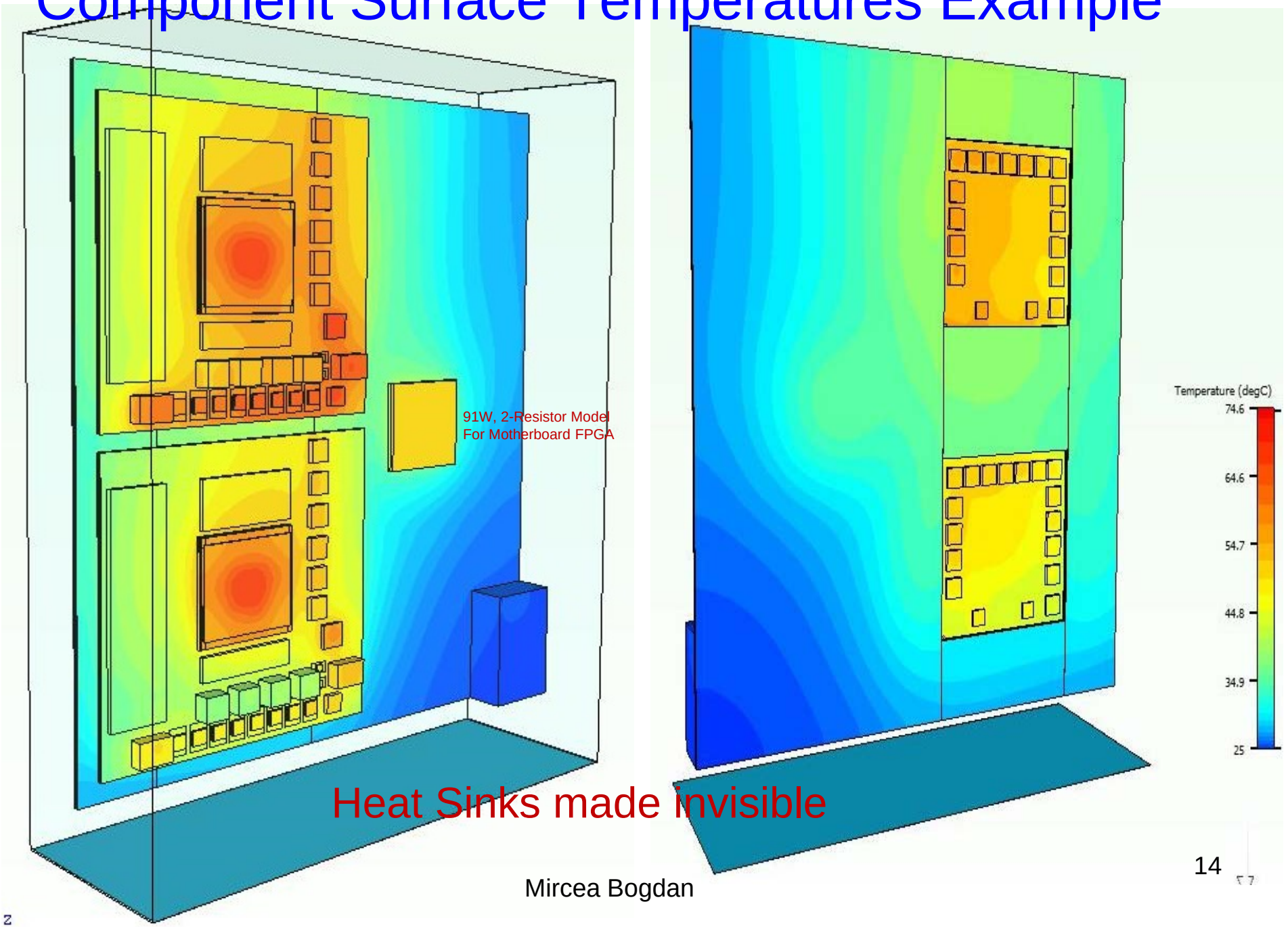
4m/s Fixed Flow from Top Out

4m/s Fixed Flow from Bottom In and from Top Out

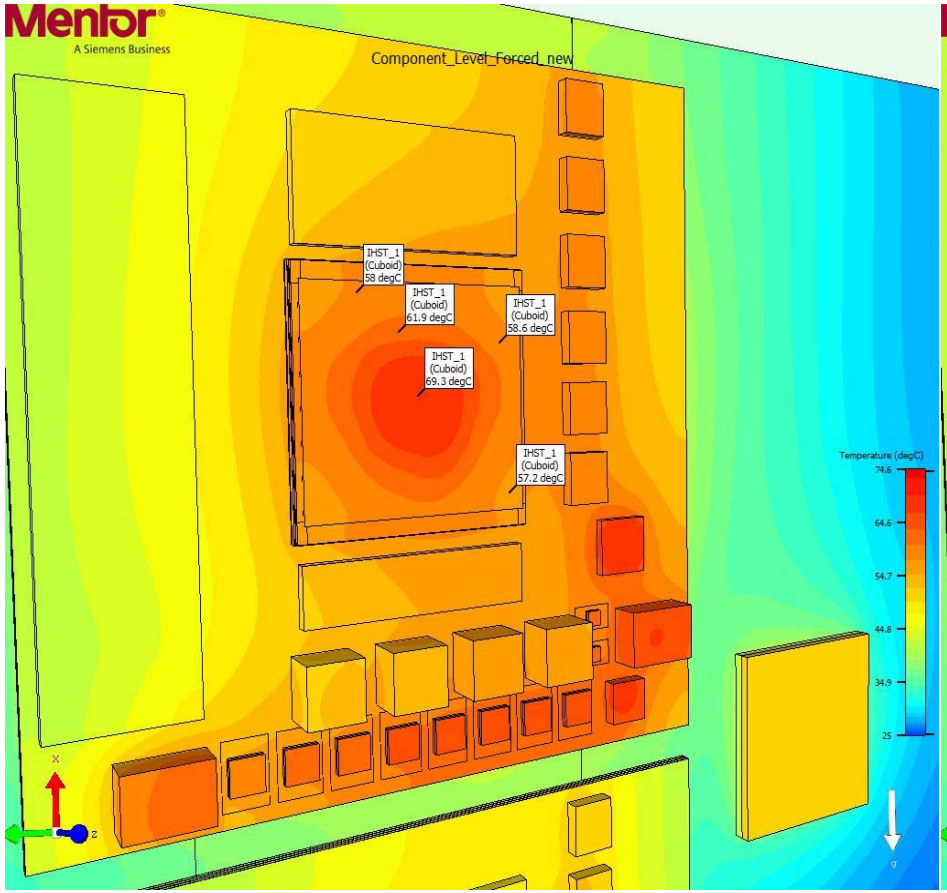


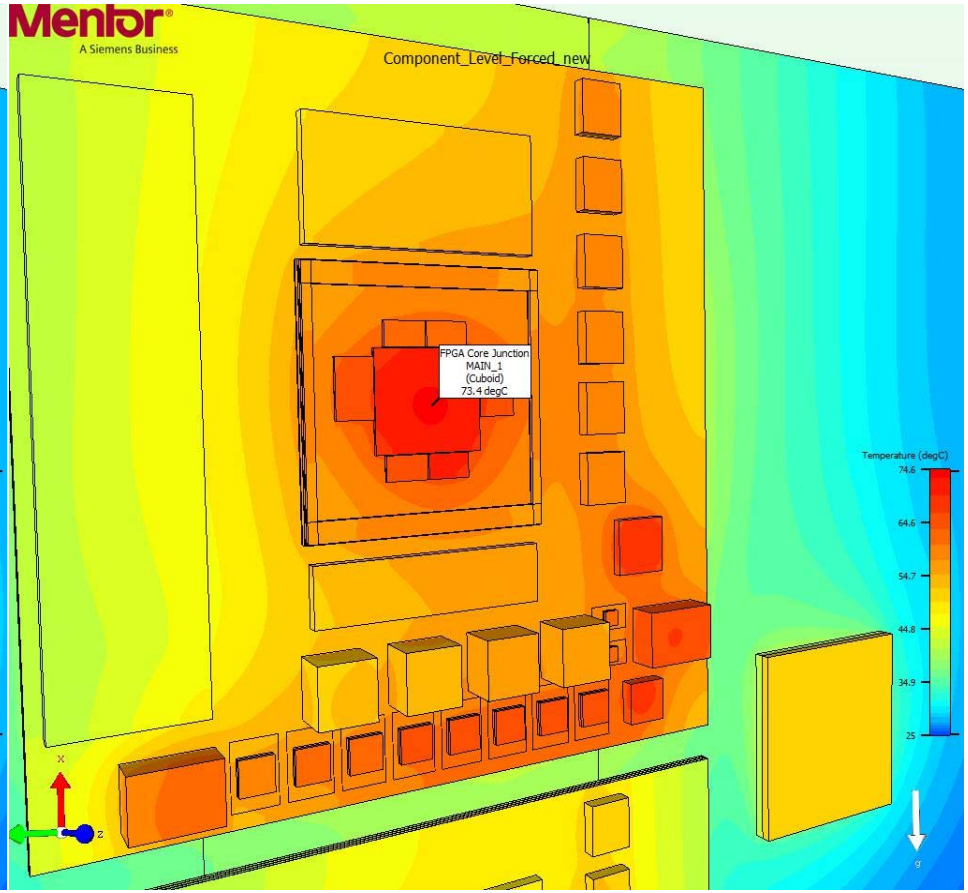
Very small local air temperature variations for the same FFSP air speed.

Component Surface Temperatures Example



Surface and Core Junction Temperatures Example - 1



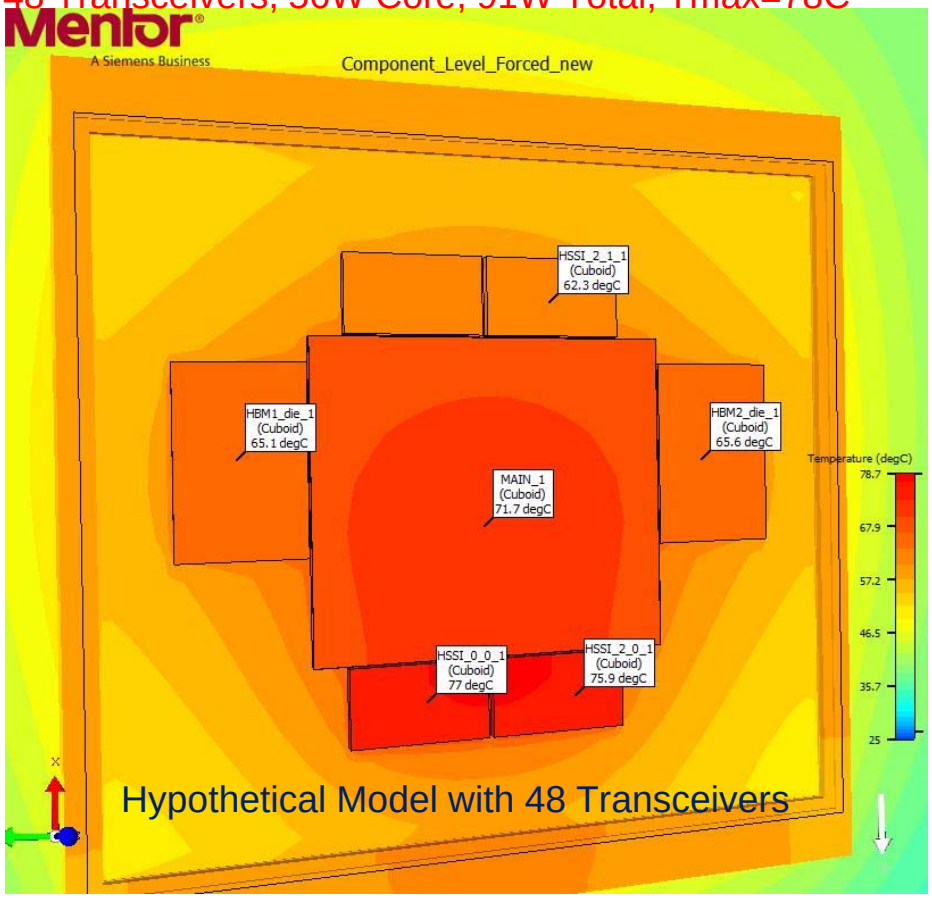


With the detailed Stratix 10Mx model for FPGA, one can check temperatures on the different dies inside.

Note: The FloTHERM simulations are not fully consistent with the original Version 18.0.1 EPE results.
This simulation shows the max temperature to be in the core.

Example: Same Cooling, Same Power -Temperature Variation with Firmware

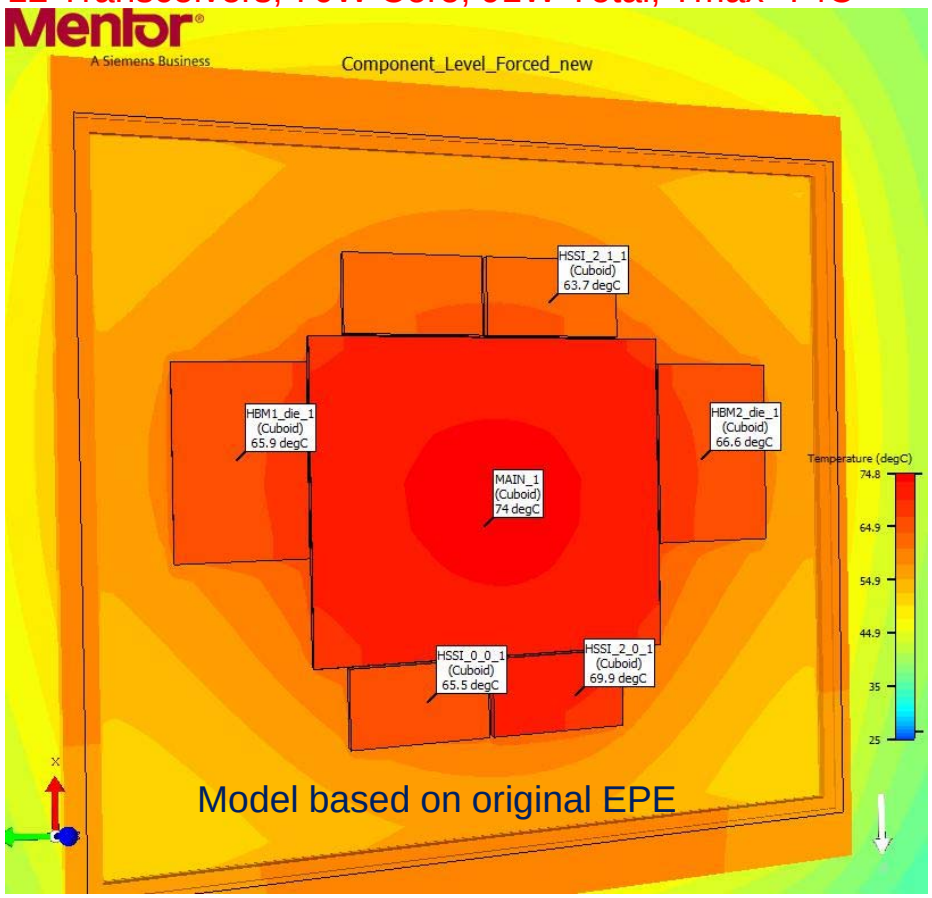
48 Transceivers, 56W Core, 91W Total, Tmax=78C



http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_2.xls

- Core	55.78W
- HBM_TOP	6.30W
- HBM_BOT	6.30W
- HSSI_2_0	11.25W
- HSSI_0_0	11.25W –> Tmax
.....	
Total	91W

12 Transceivers, 70W Core, 91W Total, Tmax=74C



http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_1.xls

- Core	70.18W –> Tmax
- HBM_TOP	6.30W
- HBM_BOT	6.30W
- HSSI_2_0	6.55W
- HSSI_0_0	1.75W
.....	
Total	91W

FPGA Max. Temperatures for Middle Blade
91W, detailed Stratix10Mx Model for Mezz FPGAs

All Simulations Solved with three Blades in Chassis, two Mezzanines on each Blade.

Mezzanine Size	74x300x21.5 2mm-Conn		150x146x21.5 2mm-Conn		74x300x21.5 0.5mm-Conn		150x146x21.5 0.5mm-Conn		170x146x21.5 0.5mm-Conn		170x164x22.5 0.5mm-Conn	
Air Flow	Right	Left	Bottom	Top	Right	Left	Bottom	Top	Bottom	Top	Bottom	Top
4m/s Push	76.68	76.68	80.30	79.08	73.07	73.21	73.95	74.13				
3m/s Push	84.43	84.37	87.46	86.58	80.03	80.23	80.28	81.09				
4m/s Push-Pull	76.41	75.77	80.05	78.50	72.77	72.61	73.68	73.47	71.25	70.60	69.28	69.32
3m/s Push-Pull							79.94	80.22	76.70	76.39	74.27	74.81
2.5m/s Push-Pull							84.64	85.39	80.79	80.82	78.05	79.01

Note: Results are based on solving the models with FloTHERM Fixed Flow Smart Parts, which were used in place of ATCA fans. The FFSP provide a uniform air speed over the entire 280x100mm section of the model chassis. In real ATCA crates, air flow varies from slot to slot and from quadrant to quadrant, in the same slot.

All Simulation Results are posted here:
http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/FloTHERM/Simulation_Results.xlsx

Comments – Questions

Requirement: 91W FPGA Power, max 80C Core Junction Temp

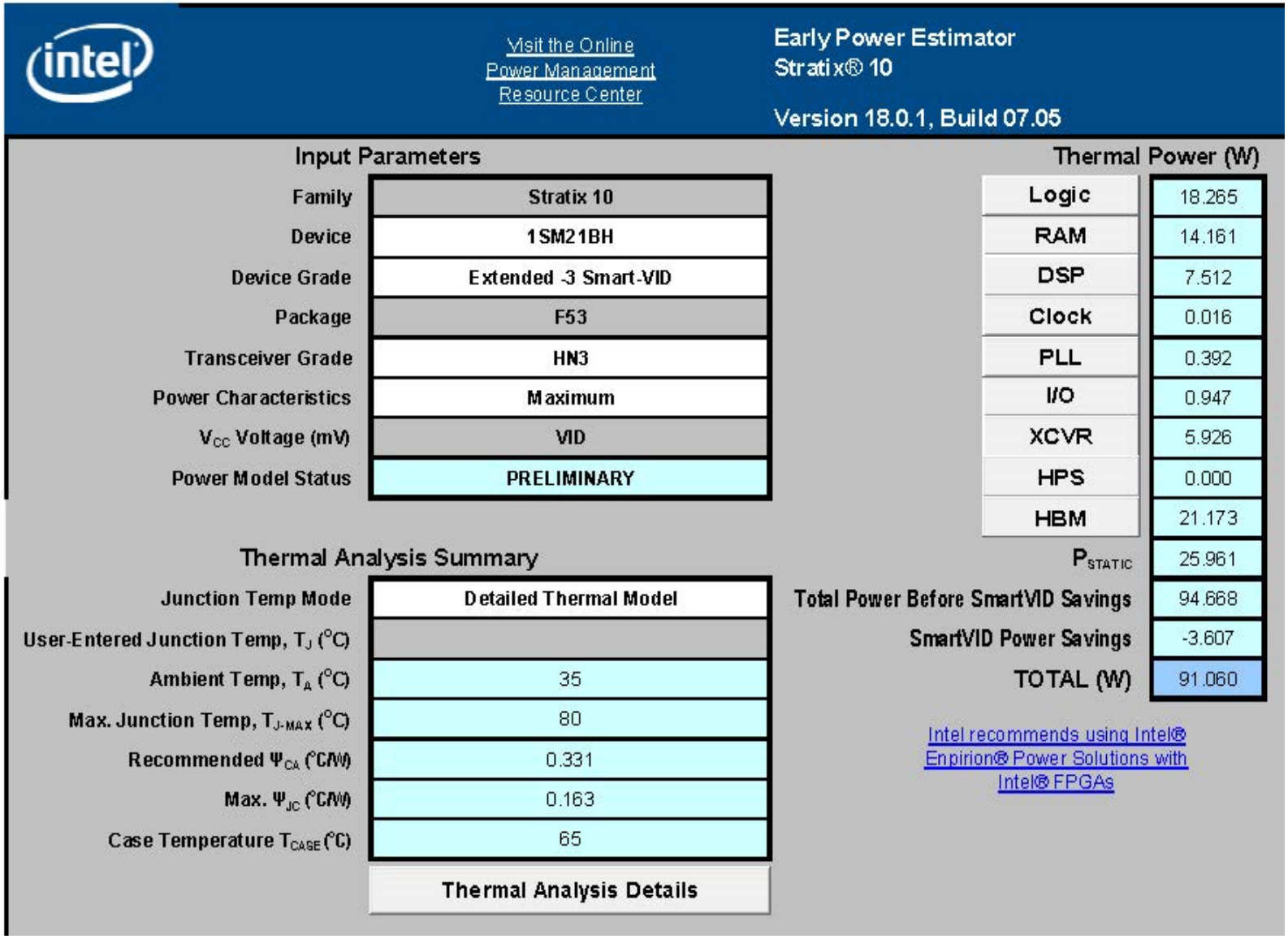
Thermal Simulations show that cooling is possible with two square mezzanine cards and 0.5mm interposers.

We have to agree about acceptable architecture: connectors, PCB geometries, PCB cutouts, etc.

It would be best to redo thermal simulation with the real PCB design, including all parts that may potentially restrict air flow, to avoid possible hot spots and confirm current results.

Backup Slides

EPE - Mezzanine FPGA - Power



Visit the Online Power Management Resource Center

Early Power Estimator
Stratix® 10

Version 18.0.1, Build 07.05

Input Parameters

Family	Stratix 10
Device	1SM21BH
Device Grade	Extended -3 Smart-VID
Package	F53
Transceiver Grade	HN3
Power Characteristics	Maximum
V_{CC} Voltage (mV)	VID
Power Model Status	PRELIMINARY

Thermal Power (W)

Logic	18.265
RAM	14.161
DSP	7.512
Clock	0.016
PLL	0.392
I/O	0.947
XCVR	5.926
HPS	0.000
HBM	21.173
P_{STATIC}	25.961
Total Power Before SmartVID Savings	94.668
SmartVID Power Savings	-3.607
TOTAL (W)	91.060

Thermal Analysis Summary

Junction Temp Mode	Detailed Thermal Model
User-Entered Junction Temp, T_J (°C)	
Ambient Temp, T_A (°C)	35
Max. Junction Temp, T_{J-MAX} (°C)	80
Recommended Ψ_{CA} (°C/W)	0.331
Max. Ψ_{JC} (°C/W)	0.163
Case Temperature T_{CASE} (°C)	65

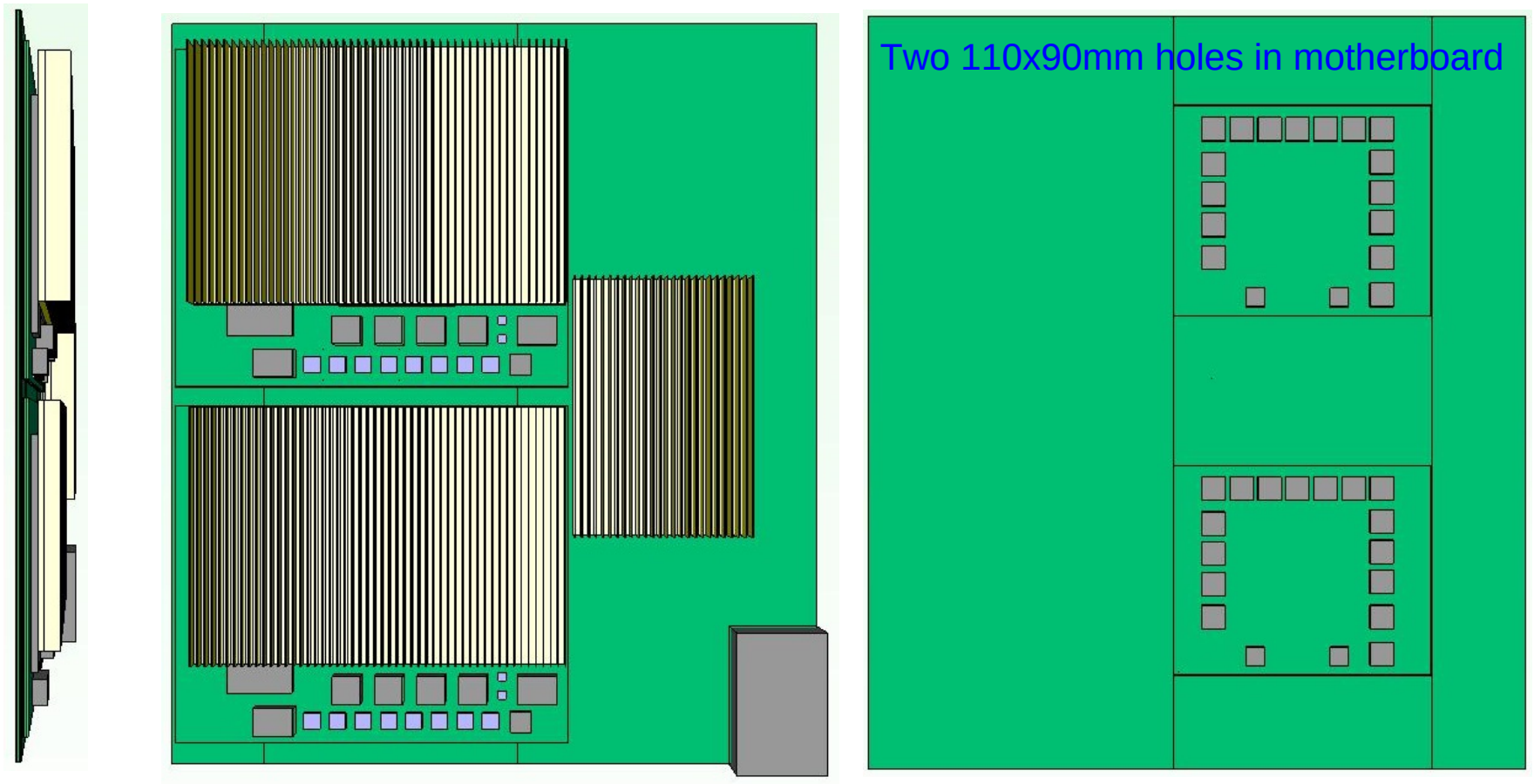
Thermal Analysis Details

Intel recommends using Intel® Enpirion® Power Solutions with Intel® FPGAs

http://edg.uchicago.edu/~bogdan/HTT_TrackFitterMezzanine/misc/stratix10_epe_TEST_1.xls

Please, Download and Test!

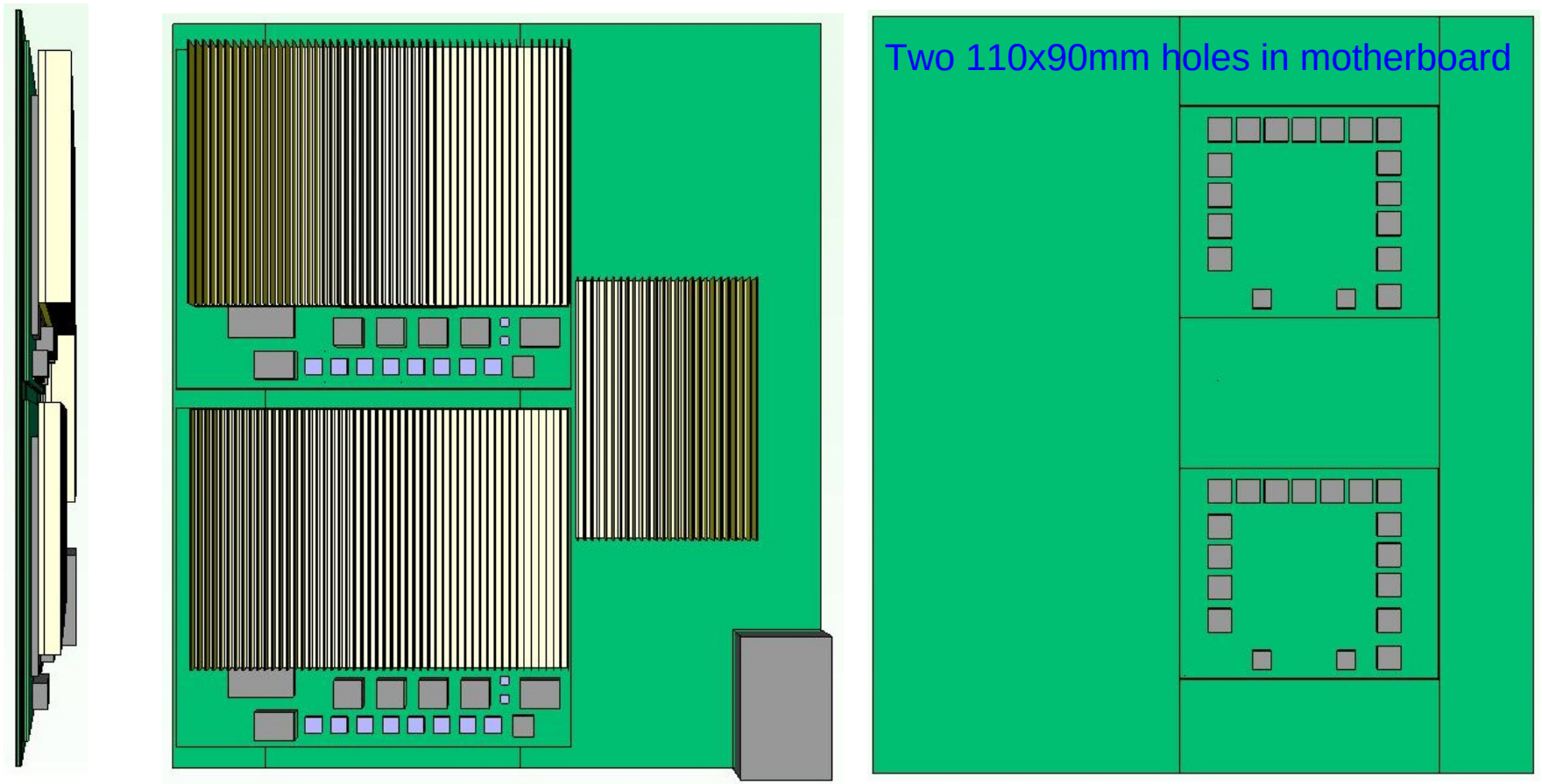
E - Larger Square Mezzanines with 0.5mm Connectors:



- Two 170x146mm Mezzanine Cards with 0.5mm Connector
- Max. Height from Motherboard Top Side : 0.5+2.5+4+3.2+11.3=21.5mm
- Heatsink Sizes:
  - Bottom Heatsink: Base = 159x110x2.7mm; 52 Fins = 0.3x110x7.3mm
  - Top Heatsink: Base = 159x110x3.2mm; 52 Fins = 0.3x110x11.3m

Mezzanine PCB Height=2.5mm, FPGA Height=4mm

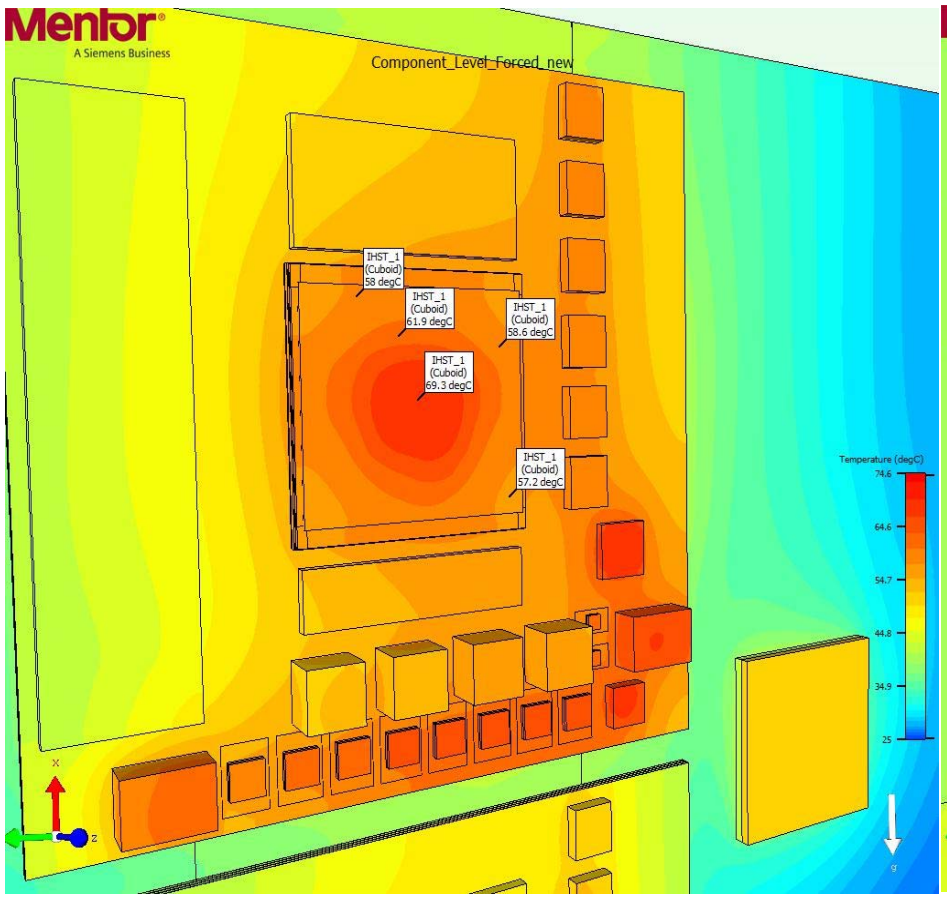
F - Larger/Taller Square Mezzanines - 0.5mm Conn:

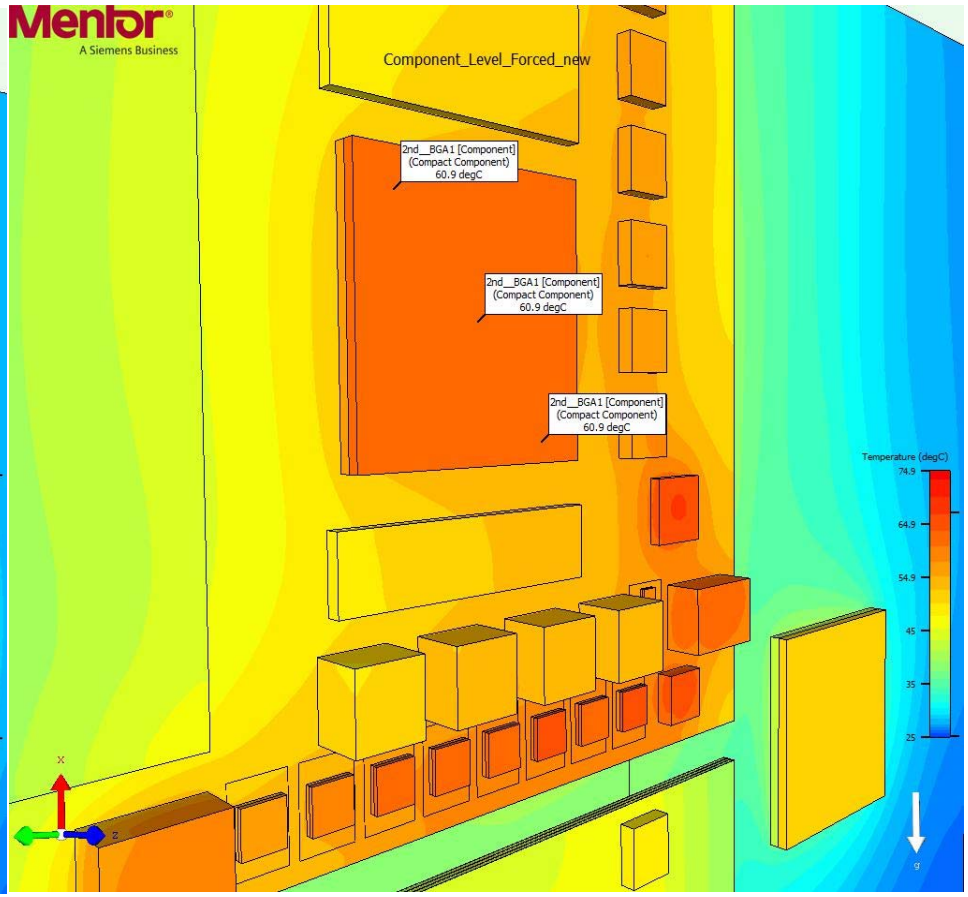


- Two 170x146mm Mezzanine Cards with 0.5mm Connector
- Max. Height from Motherboard Top Side: 0.5+2.5+4+3.2+11.3=22.5mm

  Note: Distance from Motherboard Top Side to adjacent Front Plate = 23.87mm.
- Heatsink Sizes:
  - Bottom Heatsink: Base = 159x110x2.7mm; 52 Fins = 0.3x110x8.0mm
  - Top Heatsink: Base = 159x110x3.2mm; 52 Fins = 0.3x110x12.3m

Surface and Core Junction Temperatures Example - 2





The above example shows 150x146mm cards, 21.5mm height, 0.5mm connectors and in Push 4m/s air flow.
The same Mezzanine Card was simulated with a 2-Resistor model, and a detailed Stratix 10Mx model for FPGA.

Both simulations show about the same FPGA Case Temperature of ~61C and max. junction temperature of ~74C.

FPGA Max. Temperatures for Middle Blade 91W, generic 2-Resitor Model for FPGAs

All simulations Solved with three Blades in Chassis, two Mezzanines on each Blade, pushed air

Mezzanine Size	74x300x21.5mm 2mm-Conn		150x146x21.5mm 2mm-Conn		74x300x21.5mm 0.5mm-Conn		150x164x21.5mm 0.5mm-Conn	
	Right	Left	Bottom	Top	Right	Left	Bottom	Top
FPGA Max. Temp – 4m/s	77.16	77.11	80.84	79.77	73.86	73.60	74.17	74.65
FPGA Case Temp – 4m/s	63.4	63.4	67.3	65.9	60.1	59.9	60.5	60.9
FPGA Max. Temp – 3m/s							80.46	81.52
FPGA Case Temp – 3m/s							66.9	67.7

Note: For a max. junction temperature of 80C, we need a case temperature of 65C.