Do not install Card without changing the FPGA design as follows:

- Change FPGA pin debug_8: Input for LOL.
- Change FPGA pin debug_9: Input for LOS.
- Change FPGA pin debug_5: Output driving INC.
- Change FPGA pin debug_17: Output driving 125 MHz clock.

Notes:
- Change FPGA pin debug_6: Output driving DEC.
- Change FPGA pin debug_7: Output driving RST.
- Change FPGA pin debug_8: Input for LOL.
- Change FPGA pin debug_9: Input for LOS.
- Change FPGA pin debug_10: Input for 125 MHz cleaned clock.
- Change FPGA pin debug_17: Output driving 125 MHz clock.