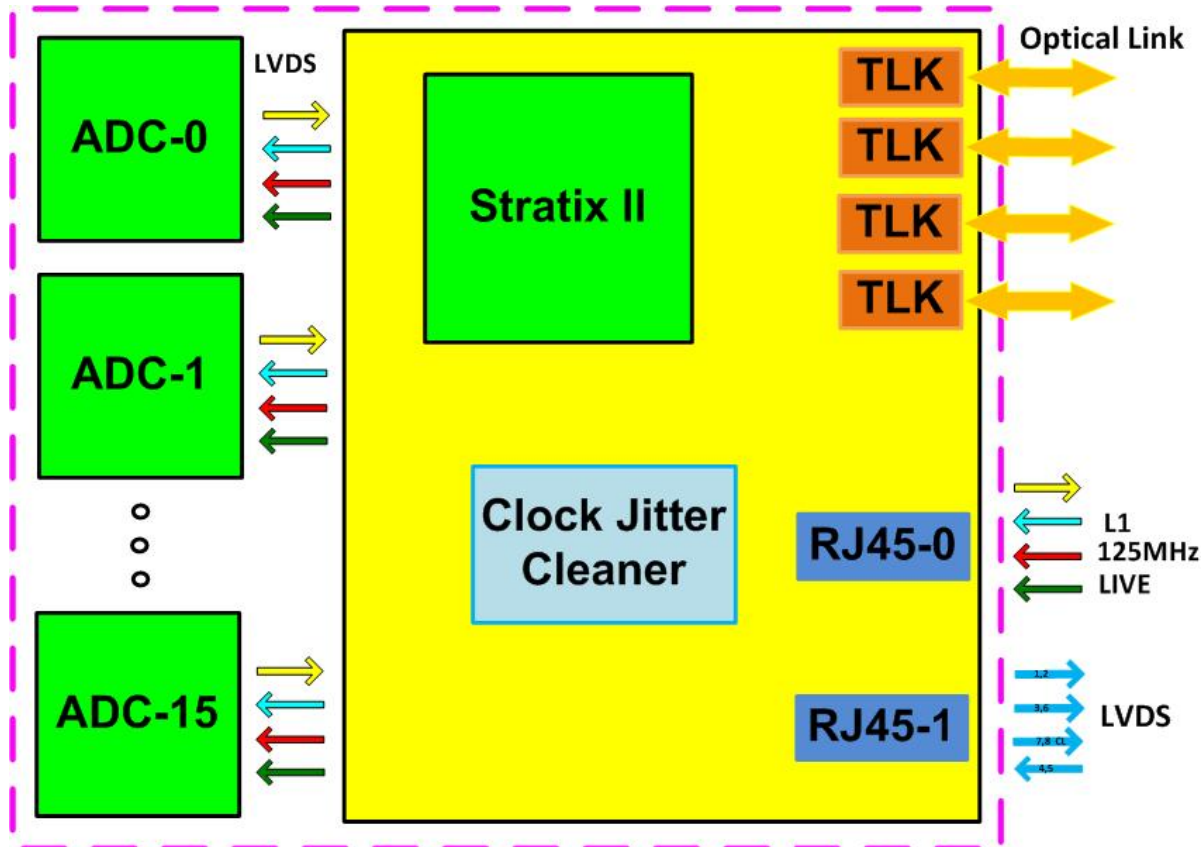# A New Clock Distribution/Topology Processor Module for KOTO (CDT)

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New CDT - Block Diagram
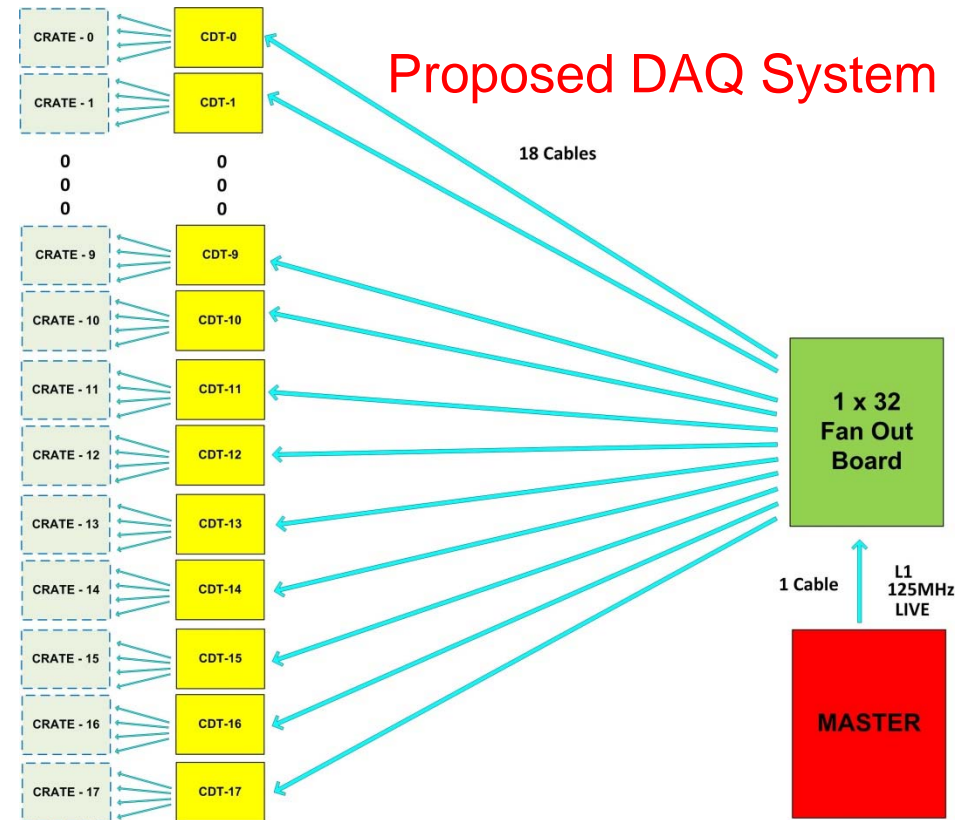

Minor changes to the Old MT Board:
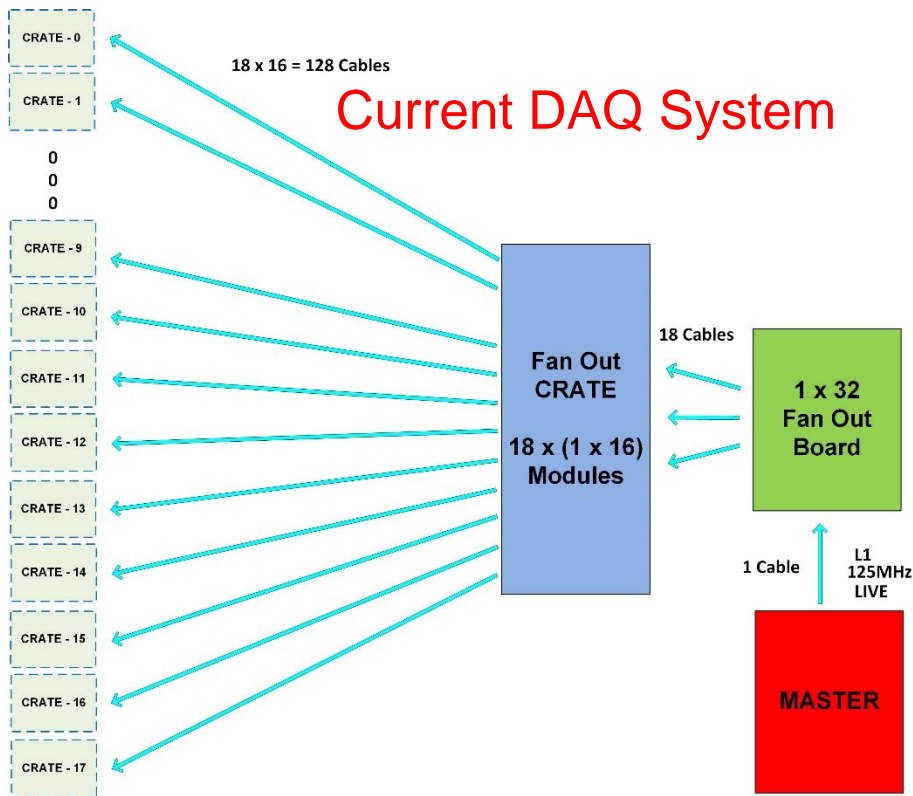- Same FPGA
- Same TLK chips

The Changes are:
- 4 TLK Chips
- 16 x RJ45 to ADCs
- 2 x RJ45 to Master
- Clock Jitter Cleaner

- 1:16 **Fan Out Card for LIVE, 125MHz Clock, L1A.**
- **Service all 16 ADCs in the Crate**
- **6U VME Double Width**

DAQ System – Old vs New

- **Insert New CDTs in the ADC Crates;**
- **Replace existing Fan Out Crate;**
- **New Jitter Cleaner will improve analog signal quality and TLK/Fiber Communication.**
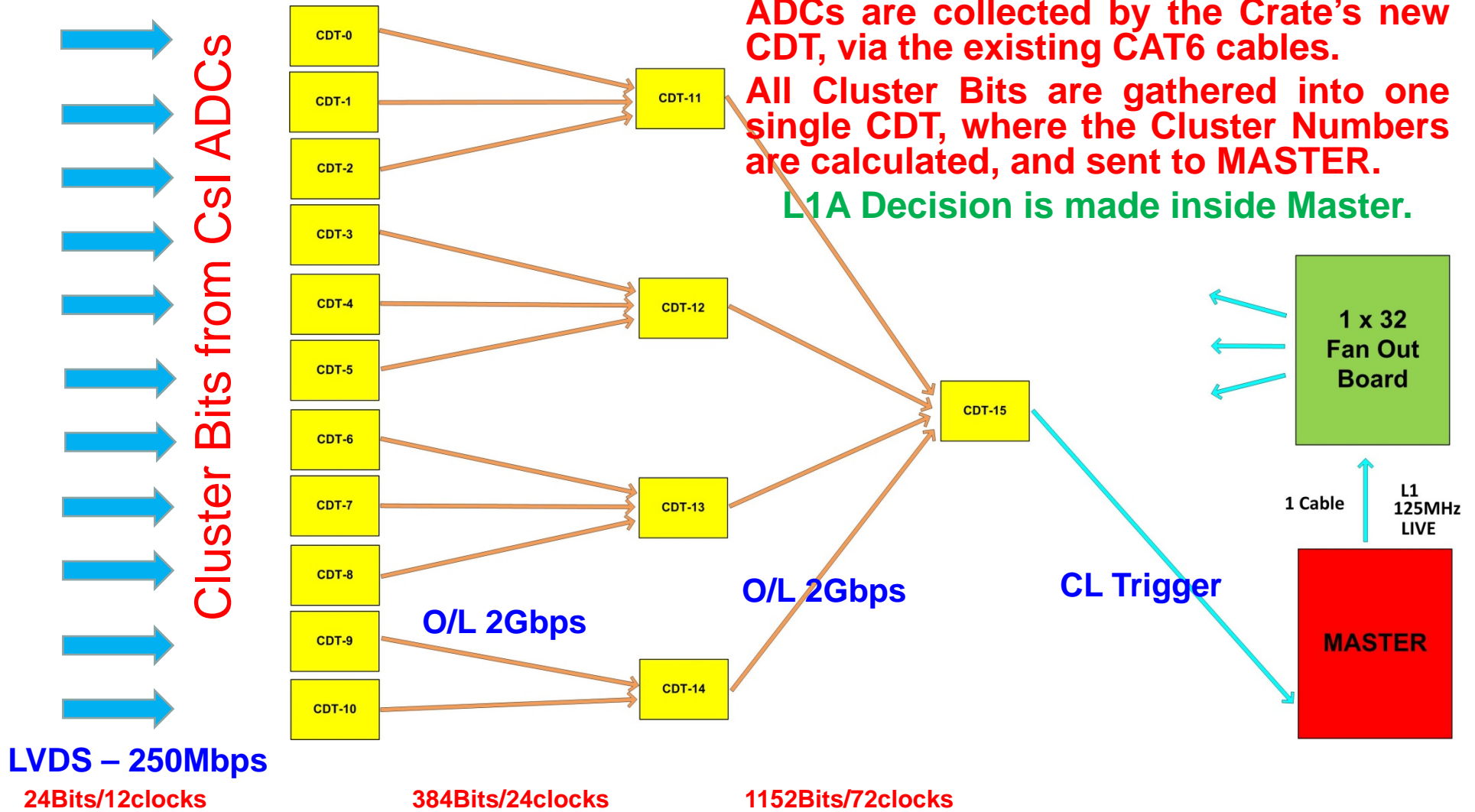
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New CDT Module Features

- **1 to 16 Fan-Out Module for 125MHz Clock, LIVE, L1A;**

- **Replaces the Fan-Out Crate with Modules placed in the ADC Crates;**

- **Jitter Cleaner: better signal integrity;**

- **Fully Compatible with Existing and Future (ATCA based) L2 System;**

- **Doesn't Require any Change in L2 Firmware or Hardware.**

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Option: CLUSTER Trigger with the new CDT Module

Before each L1A, Cluster Bits from CsI ADCs are collected by the Crate's new CDT, via the existing CAT6 cables.

All Cluster Bits are gathered into one single CDT, where the Cluster Numbers are calculated, and sent to MASTER.

L1A Decision is made inside Master.

Cluster Bits from CsI ADCs

CDT-0
CDT-1
CDT-2
CDT-3
CDT-4
CDT-5
CDT-6
CDT-7
CDT-8
CDT-9
CDT-10

CDT-11
CDT-12
CDT-13
CDT-14

CDT-15

1 x 32 Fan Out Board

1 Cable

L1 125MHz LIVE

MASTER

CL Trigger

O/L 2Gbps

O/L 2Gbps

LVDS – 250Mbps

24Bits/12clocks

384Bits/24clocks

1152Bits/72clocks

CLUSTER Trigger Function is Separate from the Fan Out

How this Cluster Trigger Works

- **A Shorter Pre-L1A pulse is sent to CsI ADCs by Master, about 300 clocks before the actual L1A pulse;**

- **ADCs calculate the Cluster Bits (one bit per channel);**

- **Currently, the RJ45 in the ADC has one LVDS Output that is not used in regular data taking.**

- **Using that LVDS Output, Cluster Bits are sent from the ADC to the CDT;**

- **From CDTs, Cluster BITS are collected into one Top CDT;**

- **Top CDT calculates Cluster Numbers and sends them to Master;**

- **Master will use Cluster Numbers to issue L1A.**

Preliminary Testing in Chicago

Can the ADCs send Cluster Data with Existing Connections?

- **Used 125MSPS ADC Modules with old MT Cards.**
- **Didn't touch the 3 lines used for Clock, LIVE, L1A.**
- **Tested ADC to MT Communication in the 4th line of the existing CAT6 Cable.**
- **Implemented SERDES Tx inside ADC FPGA: 8 BITS sent every 32ns.**
- **Implemented SERDES Rx inside MT FPGA: 8 BITS received every 32ns.**
- **One Old MT can service 8 ADCs.**

- **Tests showed reliable Data Transmission from ADC to MT at a 250MBPS Rate.**

ADC Modules are capable of sending cluster data via existing CAT6 cable

CDT Manufacturing (20 pieces) Estimate

- **Schedule:**
    - **PCB Design: 6 weeks;**
    - **PCB Manufacturing: 3 weeks;**
    - **Prototype Assembly: 3 weeks;**
    - **Production: 3 weeks.**

- **Manufacturing Cost:**
    - **PCBs - $250/piece;**
    - **Assembly: $250/piece;**
    - **Components: $1,500/piece;**
    - **Total: $2,000/piece.**

Implementation Steps

- **Test Only One New CDT Card with the rest of the System:**
  - Place CDT Card in One Crate;
  - Receive CAT6 cable from FanOut Crate and distribute Clock, LIVE, L1A to Crate;
  - One 1x16 FanOut Module is disconnected from system;
  - **No Other Change, No Firmware Change;**
  - **System should behave as before.**

- **Test NEW CDT Card in full System:**
  - Place CDT Cards in All Crates;
  - Receive CAT6 cable from 1x32 FanOut Board and distribute Clock, LIVE, L1A to Crate;
  - All 1x16 FanOut Modules are disconnected from the system;
  - **No Other Change, No Firmware Change;**
  - **System should behave as before.**

- **Test Cluster Trigger Function:**
  - Change Firmware to Include Cluster Trigger;
  - Cluster Trigger runs in parallel and with no interference with Old Style Trigger;
  - During Normal Operation, Cluster Trigger can be activated as needed.

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