Cluster Block Status Report

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Cluster Block Status Report

Manufactured 25 new CDT Modules

Tested new Modules (Yuting)

Developed Firmware for CDT:

      - CDT Block inside ADC

      - Firmware for CDT Modules (Yu-Chen)

Cluster Block Status Report

To Do in J-PARC:

      - Install new CDT Modules

      - Test Fan-Out Function
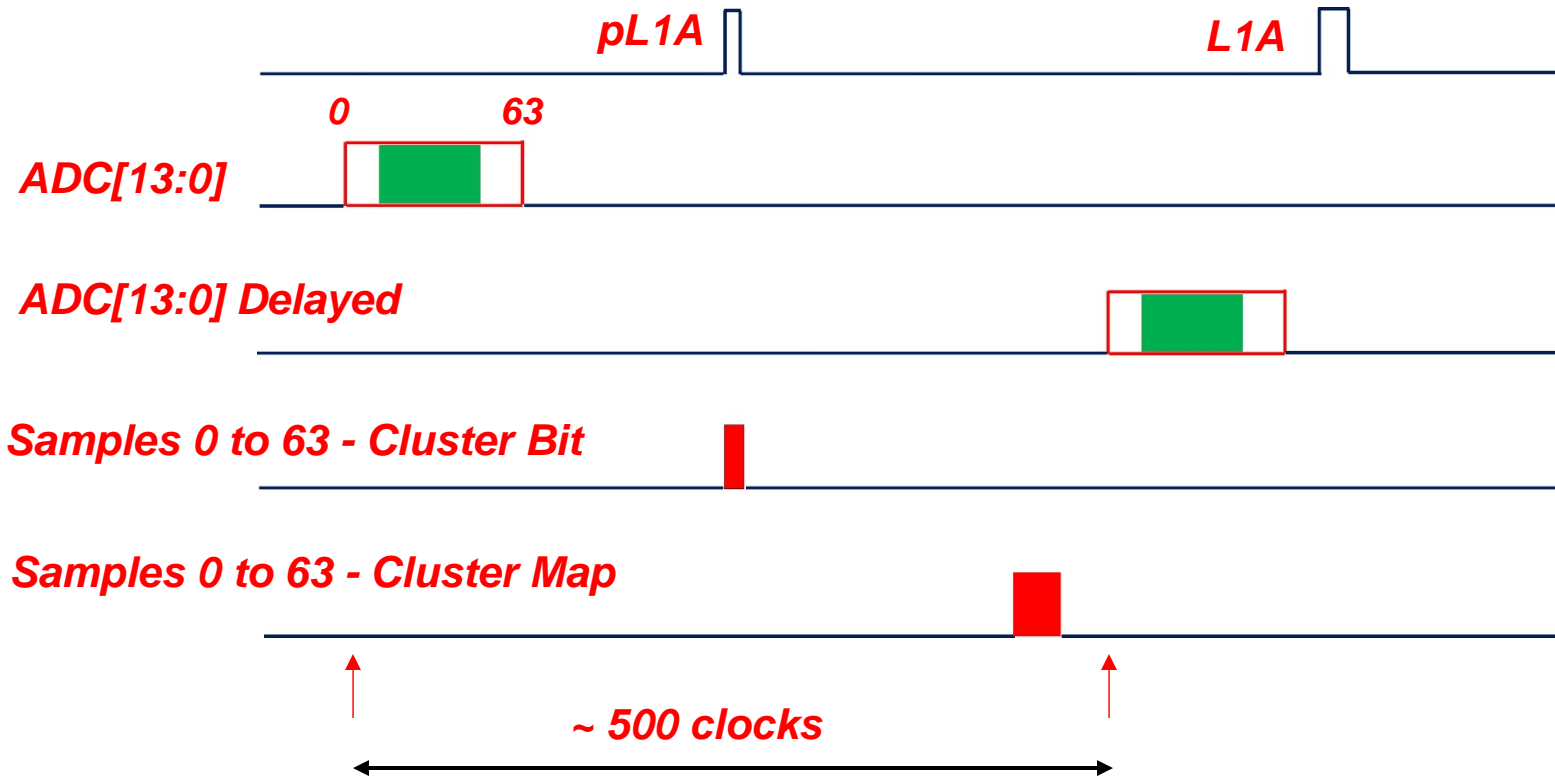
      - Test Cluster Bit Function

Collaboration:

New Blocks inside Master Firmware:
- Generation of pL1 pulse
- Management of pL1A pulse
- Receipt of Cluster Numbers. Need to finalize protocol: Cluster Numbers or Yes/No.

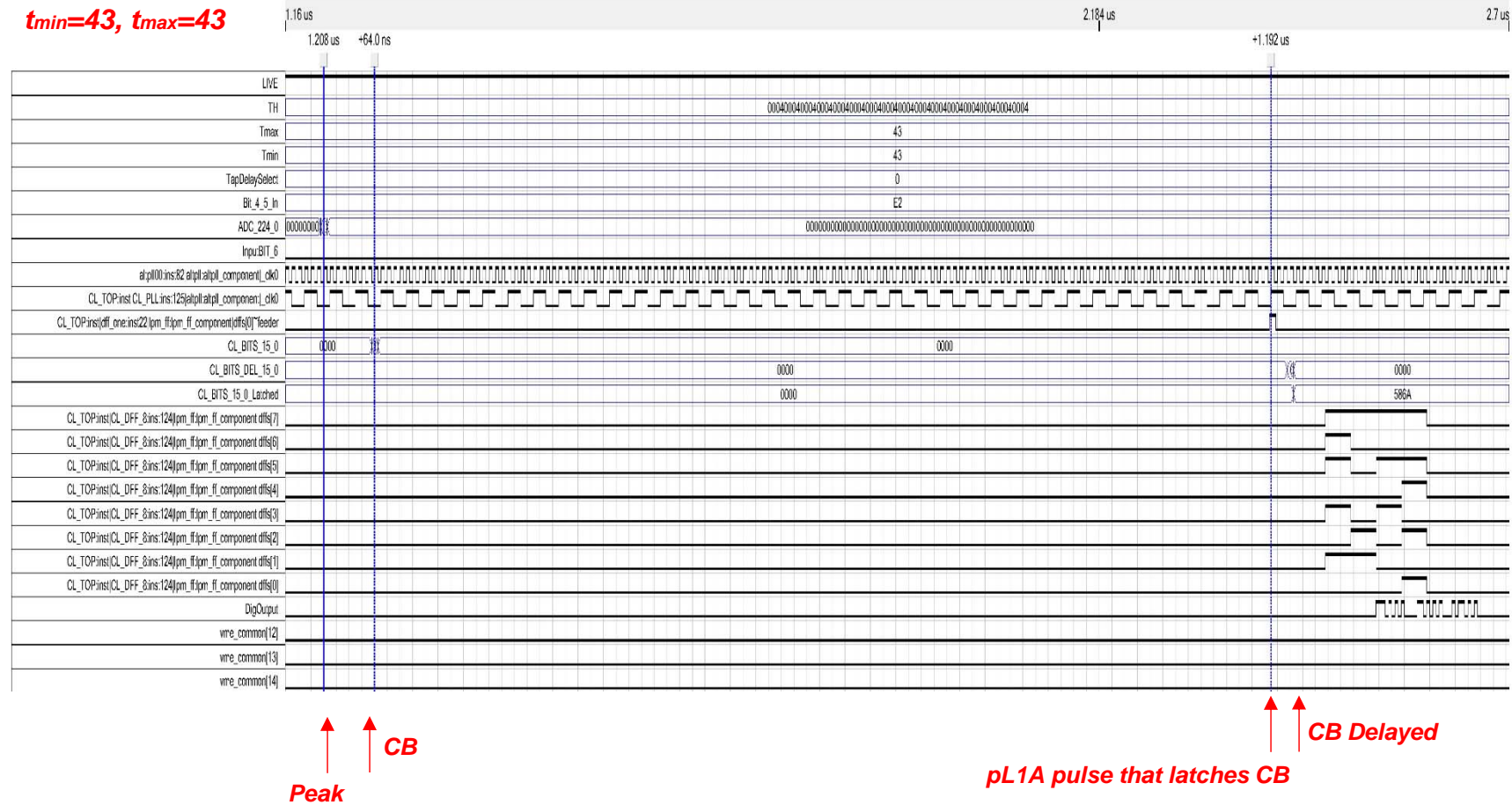Testing of CB/Master Handshake

Cluster Block Timing

Cluster Bits are calculated every 8 ns. The pL1A pulse latches the Cluster Bits corresponding to the same 64 samples that stand to produce the L1A pulse.

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Full Cluster Block Simulation

Cluster Bits are delayed.
The pL1A pulse that latches the CBs comes 150 clocks after Sample$_{43}$

Full Cluster Block Simulation - Detail
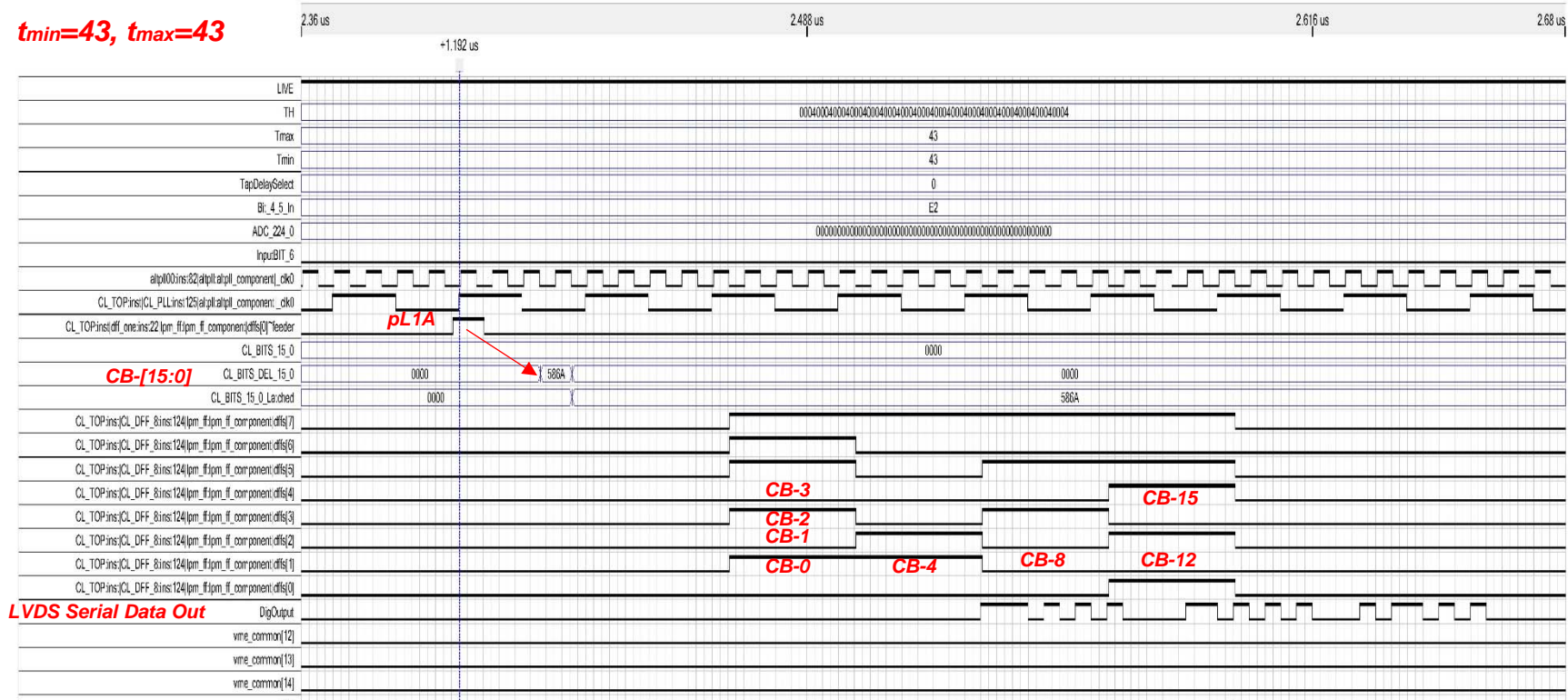
The pL1A pulse that latches delayed CBs comes 135-150 clocks after Sample[43]

One 8-Bit Bus is passed to ALTLVDS.
There are 4 successive 8-BIT Words for each trigger:
[7]= Data Valid; [6]=4-BIT Counter; [5:4]=8-BIT VME_Word; [3:0]=16 Cluster Bits.
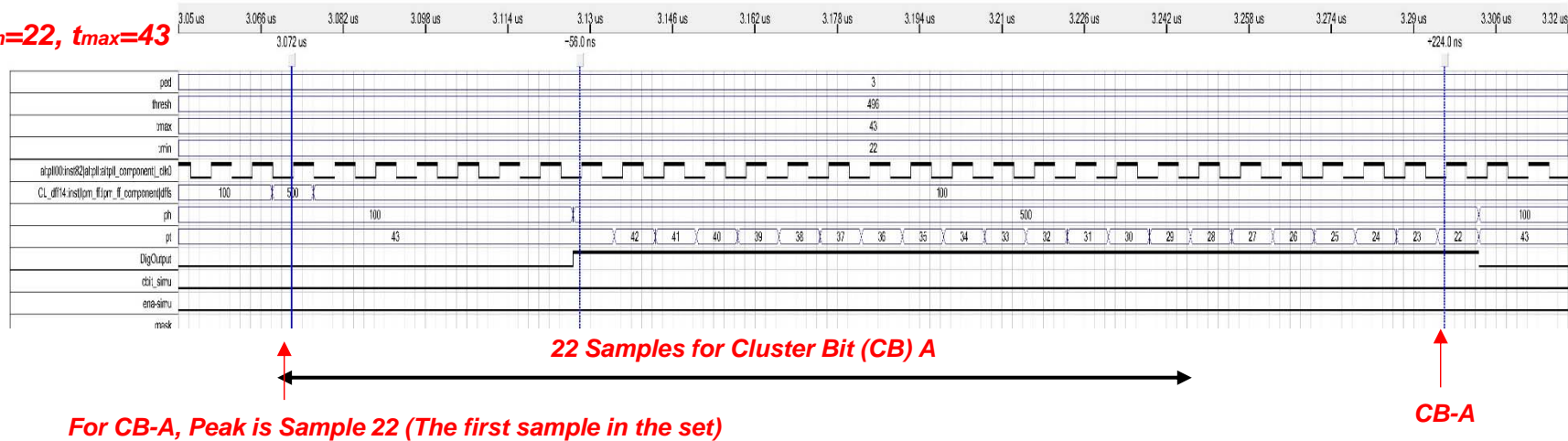
Cluster Block Simulation Examples

Backup Slides

Cluster Bit Block (CBB) Simulation Examples - A

CBB looks at 22 successive samples [22,…,43] and presents a Cluster Bit after 7 clocks.

Peak = Max Sample Value; t_{peak} = Time of Max Sample
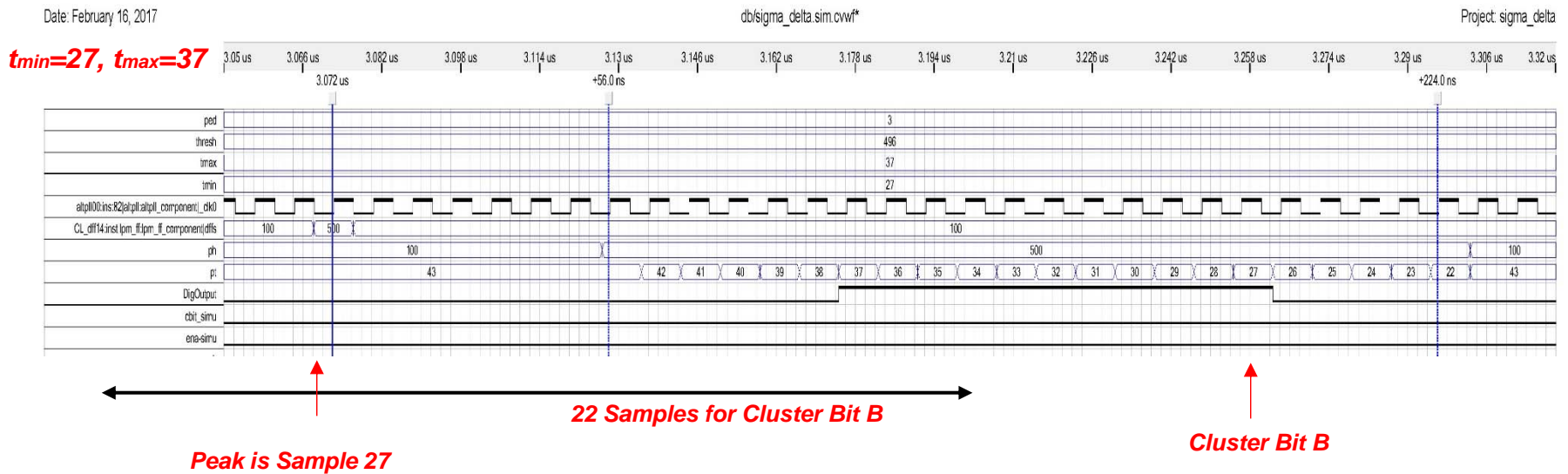
CB = 1 if Peak $\geq$ [ped(9..0) + thresh(9..0)] and $t_{min} \leq t_{peak} \leq t_{max}$

Time of each Cluster Bit: $t_{CB} = t_{Last\_sample} + 56ns.$

t_{min} and t_{max} can be set between 22 and 43.

In Example above, we have 22 successive CB=1 for one Peak.
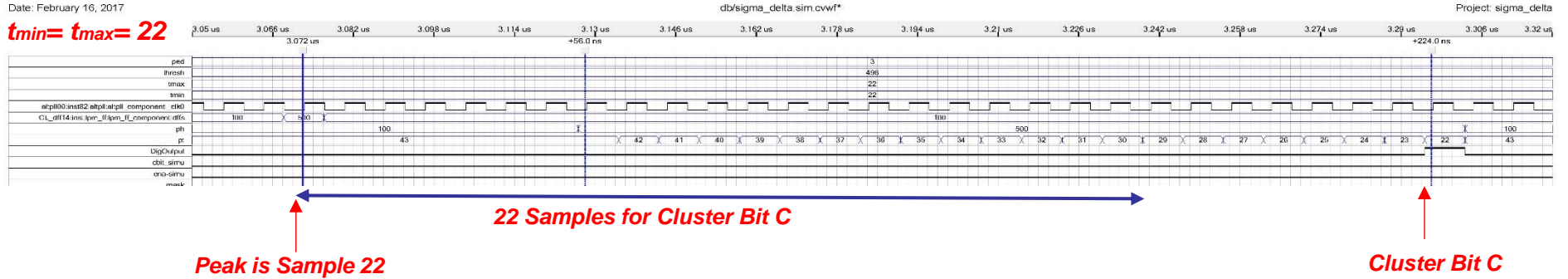
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CBB Simulation Examples - B

In this example, t_{min} = 27 and t_{max} =37, so we have 11 successive CB=1 for one Peak.
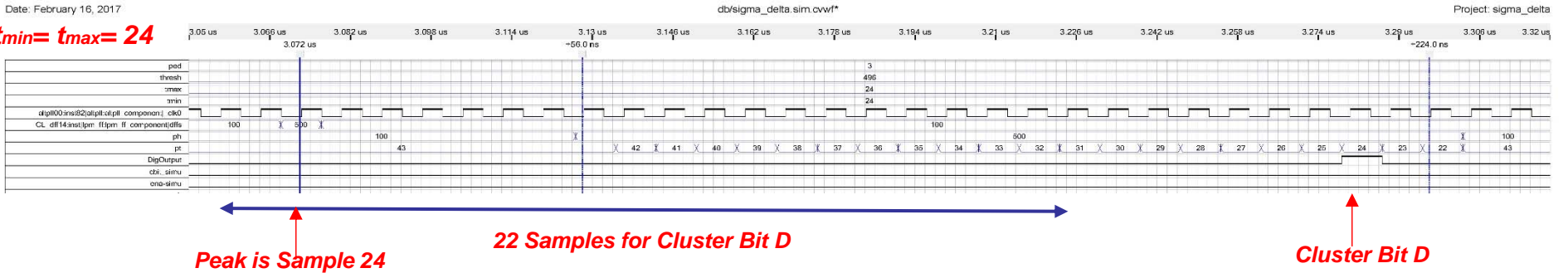
CBB Simulation Examples – C. D. E

t_{min}= t_{max}= 22

22 Samples for Cluster Bit C

Peak is Sample 22

Cluster Bit C

t_{min}= t_{max}= 24

22 Samples for Cluster Bit D

Peak is Sample 24

Cluster Bit D

t_{min}= t_{max}= 43

22 Samples for Cluster Bit E

Peak is Sample 43

Cluster Bit E

If t_{min} = t_{max} = t_m => Only one CB=1.

$t_{CB=1}$ = t_{peak} + 56ns + (43 − t_m)*8ns

Delay from Peak Moment CB=1 Moment

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