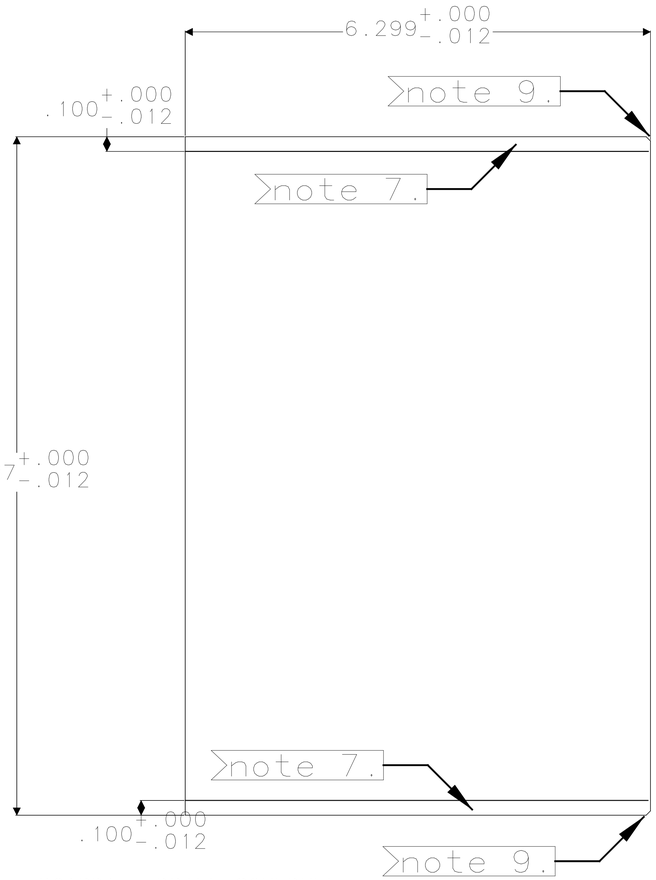

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.009	1278	YES	---	
⊞	.0091	1804	YES	---	Note 13
⊕	.014	48	YES	---	
⊟	.0181	80	YES	---	Note 11
⊖	.035	16	YES	---	
◫	.041	574	YES	---	
⊕	.0413	26	YES	---	Note 12
□	.042	20	YES	---	
	.057	6	YES	---	
	.062992126	24	YES	---	
	.073	4	YES	---	
	.106	6	NO	---	
	.12795	5	YES	---	
	.15	3	NO	---	

Board Characteristics - 16 LAYER BOARD

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
2. Minimum trace width: 0.005" and clearence: 0.005".
3. 1 oz copper for all power layers and for Top and Bottom
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5,7,10).
4. Zc=50 Ohm and Zdiff=100 Ohm for all 0.005" traces
   Perform TDR test for all signal layers.
   Present TDR test results for all signal layers.
5. Immersion Gold with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a thickness of 0.063" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Press Fit Holes with Specifications as per TE Conn. Application Specification 114-13219:
    Drilled Hole Diameter: 0.54-0.58mm
    0.46mm Ref Finished Hole Diameter After Plating
    0.025-0.050 Copper Plating (Max Hardness 150 Knoop)
    0.0001-0.0005 Au, 0.004-0.0076 Ni Immersion Gold Over Nickel (ENIG)
12. Press Fit Holes with Specifications as per TE Conn. Application Specification 114-13219:
    Drilled Hole Diameter: 1.13-1.17mm
    1.05mm Ref Finished Hole Diameter After Plating
    0.025-0.050 Copper Plating (Max Hardness 150 Knoop)
    0.0001-0.0005 Au, 0.004-0.0076 Ni Immersion Gold Over Nickel (ENIG)
13. Via in Pad - Via Fill and Overplate:
    Vias of this diameter must be completely filled with Peters PP-2795 or equivalent,
    planarized and plated over with Copper and surface finish.
    The plated cap must adhere to fill material after 1 x 550F solder shock.
14. Remove all non-functional inner layer pads for pins and vias.
15. Do Not increase size of thermal pads and associated spoke connections in holes.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	10/14/16
CHECKED M.Bogdan	10/14/16
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
KOTO - CDT Module
Specification Drawing

SIZE B | FSCM NO. | DWG. NO. 2878 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED