OFC-2 Module for KOTO

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DAQ - Block Diagram

16 ADCs_Crate-0 → 16 x 2.5Gbps → Level2-0 → 18 x 1GbE → Level2-1

16 ADCs_Crate-1

16 ADCs_Crate-17 → Level2-17
New DAQ - Block Diagram

New OFC-2 Module with 36 O/Ls

We can use more than 18 OFC1 modules, many combinations are possible in the architecture.
OFC-2 - Block Diagram

6U VME Module with 9 QSFPs and one Stratix 10Mx FPGA
1SM21BHN3F53E3VG (48 Transceivers and 8 GBytes Memory per chip)
## Intel® Stratix® 10

### INTEL® STRATIX® 10 MX (DRAM SYSTEM-IN-PACKAGE) PRODUCT TABLE

<table>
<thead>
<tr>
<th>PRODUCT LINE</th>
<th>MX 1650</th>
<th>MX 1650</th>
<th>MX 1650</th>
<th>MX 2100</th>
<th>MX 2100</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Logic elements (LEs)</td>
<td>16,790,000</td>
<td>16,790,000</td>
<td>16,790,000</td>
<td>20,733,000</td>
<td>20,733,000</td>
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<td>20,733,000</td>
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<tr>
<td>Adaptive logic modules (ALMs)</td>
<td>569,200</td>
<td>569,200</td>
<td>569,200</td>
<td>702,720</td>
<td>702,720</td>
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<tr>
<td>ALM registers</td>
<td>2,278,800</td>
<td>2,278,800</td>
<td>2,278,800</td>
<td>2,810,800</td>
<td>2,810,800</td>
<td>2,810,800</td>
<td>2,810,800</td>
<td>2,810,800</td>
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<tr>
<td>Programmable clock trees</td>
<td>8</td>
<td>16</td>
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<td>16</td>
<td>8</td>
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<tr>
<td>Hyper-regulars from intel® hyperflex™ FPGA architecture</td>
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<tr>
<td>eSRAM memory blocks</td>
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<td>eSRAM size (MB)</td>
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<tr>
<td>M20K memory blocks</td>
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<td>M20K size (MB)</td>
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<td>User memory size (MB)</td>
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<tr>
<td>18 x 18 multipliers</td>
<td>6,652</td>
<td>6,652</td>
<td>6,652</td>
<td>7,020</td>
<td>7,020</td>
<td>7,020</td>
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<tr>
<td>Peak fixed-point performance (TMACS)</td>
<td>5.3</td>
<td>5.2</td>
<td>5.2</td>
<td>6.3</td>
<td>6.3</td>
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<tr>
<td>Peak floating-point performance (TFLOPS)</td>
<td>5.3</td>
<td>5.2</td>
<td>5.2</td>
<td>6.3</td>
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</table>

### Summary:

- **All 5G/4G LTE-A/5G NR baseband encryption/authentication is implemented in-hardware.**
- **QRNG/ECDSA 256-bit/384-bit hash code authentication and channel attack protection.**

### Hardware Features:

- **Hard processor system**
- **Maximum user I/O pins**
- **LVDS pairs 1.6 Gbps (4x or TX)**
- **Total full duplex transceiver count**
- **GX1 transceiver count**
- **GX2 transceiver count**
- **PCI Express® (PCIe®) hard intellectual property (IP) blocks**
- **10G Ethernet MAC (3.2G/2.5G) hard IP blocks**
- **100G Ethernet MAC (3.2G/2.5G) hard IP blocks**
- **10 Gigabit Ethernet MAC (3.2G/2.5G) hard IP blocks**

### Package Options and I/O Pins: General-Purpose (GPP) Count, High-Voltage I/O Count, LVDS Pairs, E-Title Transceiver Count and H-Title Transceiver Count

- **Package options**
- **General-Purpose (GPP) Count**
- **High-Voltage I/O Count**
- **LVDS Pairs**
- **E-Title Transceiver Count**
- **H-Title Transceiver Count**

### Notes:

1. LE counts valid for comparing across Altera devices, but are conservative when comparing FPGAs.
2. Fixed-point performance assumes the use of fixed-point multipliers.
3. Floating-point performance is HP for completed single-precision.
4. Clock-DRM CORDIC and fast pipelining processor are available to specific Intel devices.
5. A subset of pins for each package is used for high voltage 3.3V and 2.5V interfaces.
6. All data are preliminary and subject to change without notice.

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OFC-2 Status

Work has started.