We introduce a new Optical Fiber Center (OFC) Module for the Trigger Upgrade in the KOTO Experiment at J-PARC, Japan. The KOTO DAQ consists of nearly 4,000 ADC channels over 18 crates. Running in parallel with the Total Energy (Et) based L-1 Trigger, the Cluster Trigger uses cluster bits from all 2,716 channels in the CsI detector. For each ADC channel, a number of successive samples are analyzed upon a L-1 Trigger, and a bit is set High when the peak sample is above a defined threshold. These values are calculated inside the 176 CsI-ADC modules, and collected for each crate into a Clock Distribution and Trigger (CDT) module. In the first KOTO Cluster Trigger Implementation, a 3-layer CDT pyramid scheme was employed to bring all cluster bits in one place. This new Optical Fiber Center is a 6U VME module with 18 SFP transceivers and one Intel Arria 5 FPGA. It can communicate directly with all 18 CDTs and generate a cluster map for the entire detector with minimal dead time and latency. Cluster numbers are then calculated and sent to the Trigger Master. They are used in combination with Et, for an enhanced L-1 Trigger decision.

In the KOTO experiment, the CsI Calorimeter consists of 2240 small crystals and 476 large crystals arranged in a disc shape, as shown in Figure 3. A corresponding Map of the entire CsI Detector is created for each energy based event inside the OFC Module. By utilizing an algorithm based on topology, the numbers of isolated clusters in the CsI calorimeter are calculated in real time. This Cluster Map provides information for triggering on the desired decay modes. The trigger decision can be made based on the physics of interest.

CONCLUSIONS

Five pieces OFC Module were manufactured and tested at The University of Chicago. They provide the following improvements to the DAQ:

- Reduce trigger dead-time from 100 to 18 clocks, and trigger latency from 250 to 100 clocks;
- Lower CsI Total Energy threshold, therefore increase physics sensitivity;
- Eliminate the largest systematic error (5.5%) from L1 Veto, by using OFC veto as first level veto, and allow for Veto decisions on every clock;
- Expand the capability of doing complex trigger logic and improve monitoring and debugging of the trigger system.

Provided with a powerful Intel Arria V FPGA, this module can be a useful tool for many other HEP applications.