

LVDS Repeaters
2 x FIN1104
DigIn_ADC<7:0>

Digital I/O
IO_AUX<7:0>
Sheet 3

DigIn_ADC[7:0] **LVDS: 3 x IN, 1 x OUT**

IO_AUX[7:0] **LVDS: 1 x IN, 3 x OUT**

FPGA

IO_ADC<7:0>
IO_AUX<7:0>

VME_ETC[30:0]
VME_Addr[31:2]
transceivers_OE
dir_trans
vme_data[31:0]

0_Control[7:0]
0_Tx[1:0]
0_Rx[1:0]
1_Control[7:0]
1_Tx[1:0]
1_Rx[1:0]
2_Control[7:0]
2_Tx[1:0]
2_Rx[1:0]
3_Control[7:0]
3_Tx[1:0]
3_Rx[1:0]
4_Control[7:0]
4_Tx[1:0]
4_Rx[1:0]
5_Control[7:0]
5_Tx[1:0]
5_Rx[1:0]
6_Control[7:0]
6_Tx[1:0]
6_Rx[1:0]
7_Control[7:0]
7_Tx[1:0]
7_Rx[1:0]
16_Control[7:0]
16_Tx[1:0]
16_Rx[1:0]
17_Control[7:0]
17_Tx[1:0]
17_Rx[1:0]

8_Control[7:0]
8_Tx[1:0]
8_Rx[1:0]
9_Control[7:0]
9_Tx[1:0]
9_Rx[1:0]
10_Control[7:0]
10_Tx[1:0]
10_Rx[1:0]
11_Control[7:0]
11_Tx[1:0]
11_Rx[1:0]
12_Control[7:0]
12_Tx[1:0]
12_Rx[1:0]
13_Control[7:0]
13_Tx[1:0]
13_Rx[1:0]
14_Control[7:0]
14_Tx[1:0]
14_Rx[1:0]
15_Control[7:0]
15_Tx[1:0]
15_Rx[1:0]

mem_A[22:0]
mem_B[2:0]
mem_ETC[14:0]
mem_DQ[35:0]
mem_VREF
VREF_0.9V

Sheet 6,7

VME_Interface

VME_etc[30:0]
VME_Addr[31:2]
VME_OE
VME_DIR_TRANS
Local_VME_Data[31:0]

VME_P1[159:0]
VME_P2[159:0]

Sheet 8,9,10

VTx0 VRx0
VTx1 VRx1
VTx2 VRx2
VTx3 VRx3
VTx4 VRx4
VTx5 VRx5
VTx6 VRx6
VTx7 VRx7
VTx16 VRx16
VTx17 VRx17

0_VCCCTX 0_Control[7:0] 0_Tx[1:0] 0_Rx[1:0] **Sheet 2-1**
1_VCCCTX 1_Control[7:0] 1_Tx[1:0] 1_Rx[1:0]
2_VCCCTX 2_Control[7:0] 2_Tx[1:0] 2_Rx[1:0] **Sheet 2-2**
3_VCCCTX 3_Control[7:0] 3_Tx[1:0] 3_Rx[1:0]
4_VCCCTX 4_Control[7:0] 4_Tx[1:0] 4_Rx[1:0] **Sheet 2-3**
5_VCCCTX 5_Control[7:0] 5_Tx[1:0] 5_Rx[1:0] **Sheet 2-4**
6_VCCCTX 6_Control[7:0] 6_Tx[1:0] 6_Rx[1:0] **Sheet 2-4**
7_VCCCTX 7_Control[7:0] 7_Tx[1:0] 7_Rx[1:0] **Sheet 2-4**
16_VCCCTX 16_Control[7:0] 16_Tx[1:0] 16_Rx[1:0] **Sheet 2-9**
17_VCCCTX 17_Control[7:0] 17_Tx[1:0] 17_Rx[1:0]

VTx8 VRx8
VTx9 VRx9
VTx10 VRx10
VTx11 VRx11
VTx12 VRx12
VTx13 VRx13
VTx14 VRx14
VTx15 VRx15

8_Control[7:0] 8_Tx[1:0] 8_Rx[1:0] **Sheet 2-5**
9_Control[7:0] 9_Tx[1:0] 9_Rx[1:0]
10_Control[7:0] 10_Tx[1:0] 10_Rx[1:0] **Sheet 2-6**
11_Control[7:0] 11_Tx[1:0] 11_Rx[1:0]
12_Control[7:0] 12_Tx[1:0] 12_Rx[1:0] **Sheet 2-7**
13_Control[7:0] 13_Tx[1:0] 13_Rx[1:0]
14_Control[7:0] 14_Tx[1:0] 14_Rx[1:0] **Sheet 2-8**
15_Control[7:0] 15_Tx[1:0] 15_Rx[1:0]

VIO_1.8V VIO_2.5V VTT_0.9V VDDQ_1.8V

VDD_1.8V VEXT_2.5V VTT_0.9V VDDQ_1.8V

A[22:0]
B[2:0]
ETC[14:0]
DQ[35:0]
VREF

RAM
Sheet 4

Power

+5V
+3.3Vin
GND

Sheet 5

P0[94:0]

Engineer: M. Bogdan	<i>Optical Fiber Center Module</i> Top Level The University of Chicago
Drawn by: M. Bogdan	
DATE: 6/28/17	
SPC#2902 ASM#2903	REV. A DRW. 2901 Sheet 1