+1.2Va	1 VDD1	+1.2Va	31 VDD4
GND	2 CHAN5sel		32 D10
GND	3 RD5		33 D11
GND	4 GND1	+1.2Va	34 V2GP
GND	5 COMPptest	chanROmonitor	35 chanROmonitor
+1.2Va	6 COMPntest	GND	36 V2GN
	7 COMPouttest		37 ROmonitor
GND	8 BUFintest	GND	38 GND6
	9 BUFouttest	GND	39 RD4
GND	10 NC		40 TRIGout4
GND	11 GND2	+1.2Va	41 VDD5
GND	12 TOKin2	GND	42 RD3
	13 TOKout2		43 TRIGout3
GND	14 GND3	GND	44 GND7
CLEARglob	15 CLEARglob2		45 SWvar_obsv
+1.2Va	16 VDD2	GND	46 GND8
GND	17 RdClk2	Mclk	47 MClk
GND	18 GND4	+1.2Va	48 VDD6
	19 D0	SWfixed_obsv	49 SWfixed_obsv
	20 D1	GND	50 GND9
	21 D2	+1.2Va	51 VDD7
	22 D3		52 TRIGout2
+1.2Va	23 VDD3	GND	53 RD2
	24 D4	GND	54 GND10
	25 D5	TRIGdelay_out	55 TRIGdelayout1
	26 D6	TRIGout	56 TRIGout1
	27 D7	Rd	57 RD1
	28 D8	58_CEXT	58 CEXT
	29 D9	59_RAMPbias	59 RAMPbias
GND	30 GND5	GND	60 GND11

+1.2Va	61 VDD8	GND	91 GND17
TRIG_ext	62 TRIGext	+1.2Va	92 ANALOGout_select
GND	63 GND12	TOKtime_sel	93 TOKtime_select
	64 RAMPbufferout	GND	94 GND18
+1.2Va	65 RAMP	signal1	95 signal1
CLEARglob	66 CLEARglob1	DACoutone_0	96 vbias1
GND	67 TRIGtr4	GND	97 GND19
GND	68 TRIGtr3	+1.2Va	98 VDD13
GND	69 TRIGtr2	GND	99 signal2
DACoutone_1	70 TRIGtr1	GND	100 vbias2
+1.2Va	71 VDD9	DACouttwo_1	101 VCP
72_TRIGbias	72 TRIGbias	GND	102 GND20
GND	73 GND13	VDLout	103 VDLout
RDclk1	74 RdClk1	GND	104 GND21
GND	75 GND14	DACouttwo_0	105 VCN
TOKout	76 TOKout1	GND	106 vbias3
TOKin	77 TOKin1	GND	107 signal3
+1.2Va	78 VDD10	+1.2Va	108 VDD14
GND	79 GND15	GND	109 GND22
CHAN_select	80 CHANselect0	GND	110 vbias4
GND	81 CHANselect1	GND	111 signal4
GND	82 TRIGdelay_cntrl	GND	112 GND23
TRIG_mode	83 TRIGmode	+1.2Va	113 VDD15
TRIG_sign	84 TRIGsign	+1.2Va	114 VswP
+1.2Va	85 VDD11	GND	115 VswN
TOKblock_select_1	86 TOKblocksel1	+1.2Va	116 VDD16
TOKblock_select_0	87 TOKblocksel0		117 REStestp
GND	88 GND16		118 REStestn
Analog_Output	89 ANALOGout		119 PROBEpowclamp
+1.2Va	90 VDD12	GND	120 GND24

Flip1
ASIC1_flip

Writeclocks[1:0]
0 VDLout
1 Mclk

StartADC[10:0]
0 TRIGout
1 TRIGdelay_out
2 Rd

SelectControls[6:0]
0 CHAN_select
1 TOKblock_select_0
2 TOKblock_select_1
3 TOKtime_sel

ReadCtrl[5:0]
0 RDclk1
1 TOKin
2 TOKout

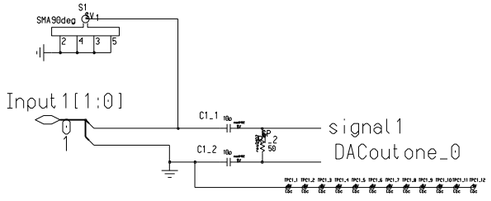
Aux[5:0]
0 SWfixed_obsv
1 chanROmonitor
2 CLEARglob

Trigger[2:0]
0 TRIG_mode
1 TRIG_ext
2 TRIG_sign

Analog_Output
Analog_Output

DACoutone[1:0]
0 DACoutone_0 *pin_96 - vbias1*
1 DACoutone_1 *pin_70 - TRIGtr1*

DACouttwo[1:0]
0 DACouttwo_0 *pin_105 - VCN*
1 DACouttwo_1 *pin_101 - VCP*

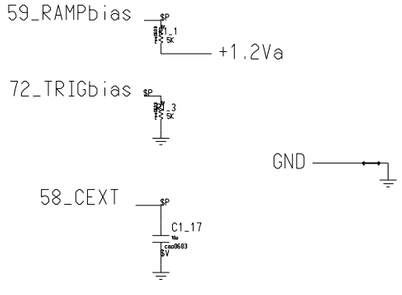


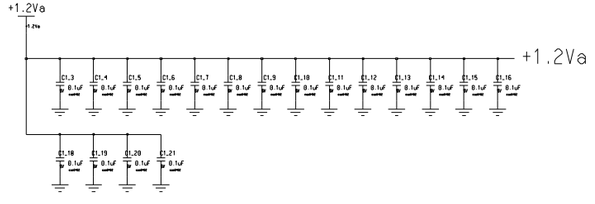
Input2[1:0]

Input3[1:0]

Input4[1:0]

Ch 2,3,4 are not used.





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Drawn by	M.Bogdan		
R&D CHK		TITLE *ASIC* *PSEC2 Flip Chip ADC Module*	Size C
DATE:	8/16/10		
TIME:	2:00 pm		
QA CHK		REV A	DRW. 2707	Sheet 3 of 7