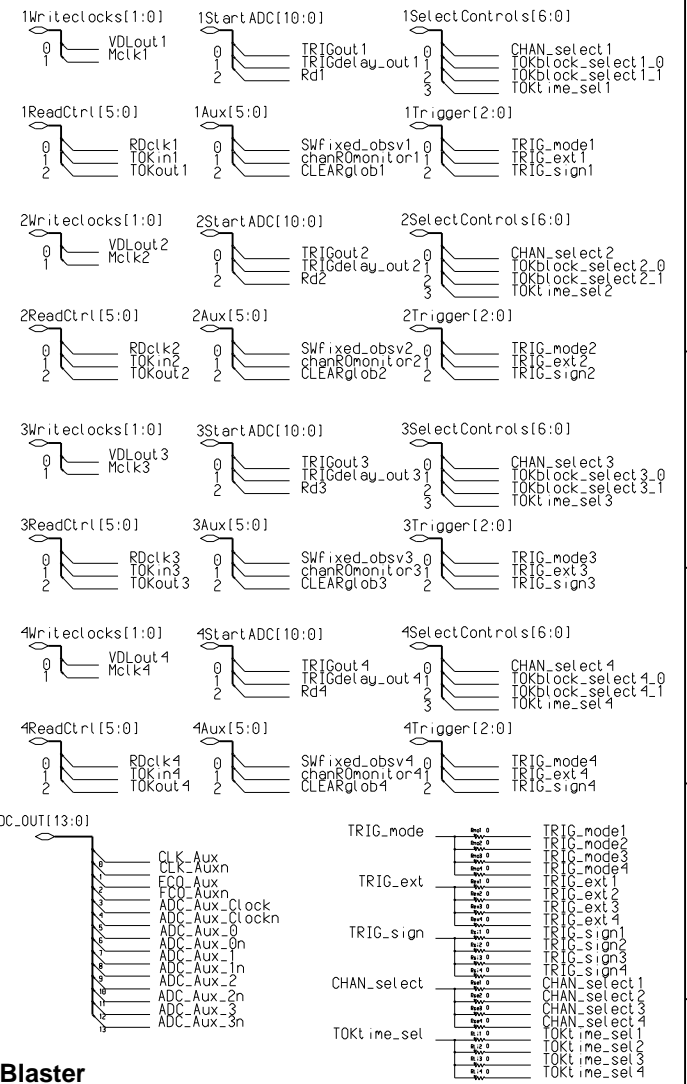
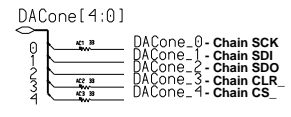
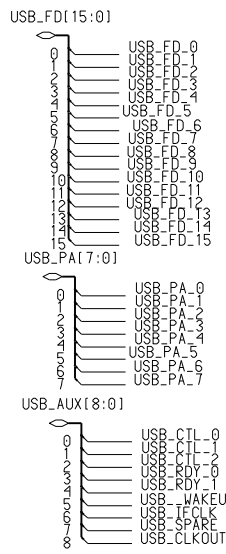
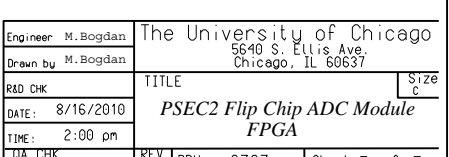
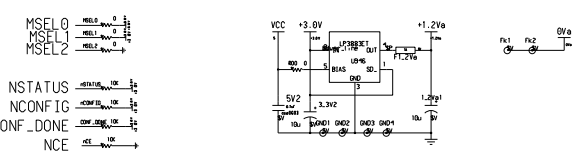
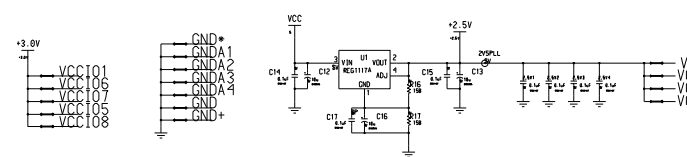
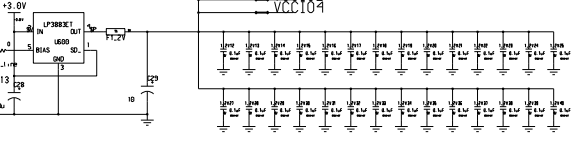
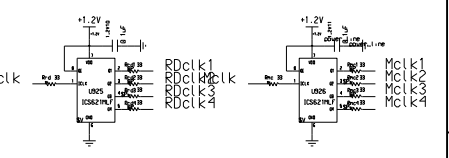
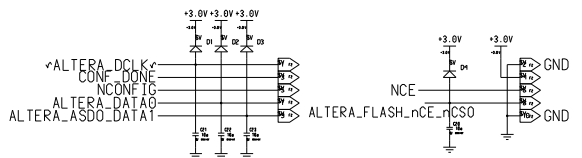
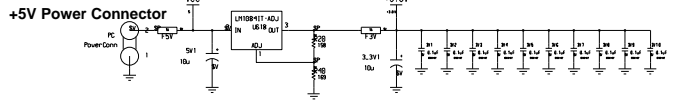
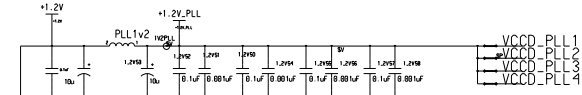
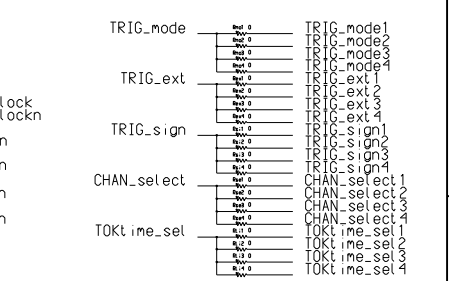
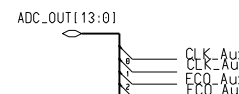
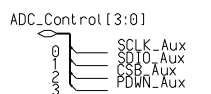
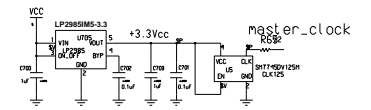
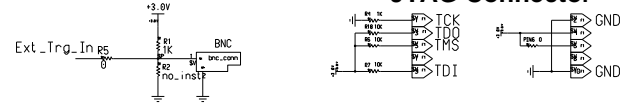


VCCD_PLL3	VCCD_PLL3ADC_Aux_1	10.4	TRIGdelay_out4	10.81	VCCD_PLL4	VCCD_PLL4.121	TOK_in2	10.161	USB_FD_5	10.201	
GND	GND	GND.42	TOK_in3	10.82	GND	GND	GND	GND	GND	GND	
VCCA3	VCCA3.3ADC_Aux_1n	10.43	VDLout3	10.83	VCCA4	VCCA4.123	VCCINT	VCCINT.163	USB_CTL_0	10.203	
CLK_Aux	10.4	ADC_Aux_0	10.4	chanR0monitor4	10.84	VCC105	VCC105.124	VDLout2	10.164	VCCINT	VCCINT.204
CLK_Auxn	10.5	ADC_Aux_0n	10.45	VCCINT	VCCINT.85	GND	GND.125	GND	GND.165	GND	GND.205
GND*	10.6	GND*	10.46	GND	GND.86	Rd3	10.126	SWFixed_obsv4	10.166	VCC107	VCC107.206
VCC101	VCC101.7	VCC102	VCC102.47	Rd2	10.87	TOKout3	10.127	VDLout4	10.167	USB_FD_8	10.207
GND	GND.8	GND	GND.48	CLEARglob3	10.88	TOK_in1	10.128	TOKblock_select1.1	10.168	GND	GND.208
debug2v5_13	10.9	ADC_Aux_2	10.49	TOKout2	10.89	VCCINT	VCCINT.133	TOKblock_select2.1	10.169	GND+	CLK8.209
VCCINT	VCCINT.ADC_Aux_2n	10.5	chanR0monitor3	10.84	CLK14.90	GND	GND.130	VCC106	VCC106.170	GND+	CLK9.210
GND	GND.11	GND*	10.51	ADC_Aux_Clock	10.89	TRIG_ext	10.131	TOKblock_select2.0	10.171	GND+	CLK10.211
ALTERA_ASIO_DATA1	10.12	GND*	10.5	ADC_Aux_Clockn	10.92	TRIGout3	10.132	GND	GND.172	GND+	CLK11.212
debug2v5_12	10.13	VCCINT	VCCINT.53	GND*	10.5	TOKblock_select3.0	10.173	VCC108	VCC108.213		
ALTERA_FLASH_nCE_nCS0	10.14	GND	GND.54	GND*	10.94	TRIGdelay_out1	10.134	VCCINT	VCCINT.174	USB_PA_0	10.214
VCC101	VCC101.debug2v5_14	10.55	GND*	10.95	SWFixed_obsv2	10.135	GND	GND.175	GND	GND.215	
GND	GND.18	debug2v5_4	10.56	VCC104	VCC104.96	VCC105	VCC105.133	CHAN_select	10.176	USB_PA_7	10.216
nSTATUS	nSTATUS.debug2v5_15	10.57	GND	GND.97	chanR0monitor1	10.137	TOKtime_sel	10.177	USB_PA_3	10.217	
GND*	10.18	VCCA1	VCCA1.5	debug2v5_11	10.98	GND	GND.138	VCCA2	VCCA2.178	USB_FD_3	10.218
VCCINT	VCCINT.19	GND	GND.54	debug2v5_10	10.99	CLEARglob1	10.139	GND	GND.179	USB_FD_0	10.219
GND	GND.20	VCCD_PLL1	VCCD_PLL1.debug2v5_5	10.100	VCCINT	VCCINT.140	VCCD_PLL2	VCCD_PLL2.180	VCCINT	VCCINT.220	
FCO_Aux	10.21	VCCINT	VCCINT.61	VCCINT	VCCINT.101	GND	GND.141	DACon0_0	10.181	USB_FD_4	10.221
FCO_Auxn	10.22	GND	GND.62	GND	GND.102	SWFixed_obsv3	10.142	DACon0_3	10.182	GND	GND.222
ALTERA_DCLK	TOKblock_select4.1	10.63	debug2v5_6	10.103	TRIGdelay_out3	10.143	DACon0_4	10.183	USB_FD_12	10.223	
ALTERA_DATA0	10.24	Rd4	10.64	VCC104	VCC104.104	chanR0monitor2	10.144	DACon0_2	10.184	USB_RDY_1	10.224
nCONFIG	TOKblock_select4.0	10.65	GND	GND.105	CLEARglob2	10.145	DACon0_1	10.185	VCC108	VCC108.225	
TDI	101.26	VCC103	VCC103.debug2v5_8	10.106	TOKblock_select3.1	10.146	USB_PA_4	10.186	USB_FD_14	10.226	
TCK	101.27	GND	GND.67	debug2v5_7	10.107	TRIG_mode	10.147	USB_FD_15	10.187	GND	GND.227
TMS	101.28	TOK_in4	10.68	debug2v5_3	10.108	TRIG_sign	10.148	led_1	10.188	VCCINT	VCCINT.228
TDO	101.29	Mclk	10.69	debug2v5_9	10.109	GND+	CLK7.149	USB_IFCLK	10.189	GND	GND.229
nCE	nCE.30	CLEARglob4	10.70	debug2v5_0	10.110	GND+	CLK6.150	VCCINT	VCCINT.190	USB_CTL_2	10.230
master_clock	CLK0.31	TOKout1	10.71	debug2v5_1	10.111	SWFixed_obsv1	10.151	GND	GND.191	USB_RDY_0	10.231
GND+	CLK1.32	Rd1	10.72	debug2v5_2	10.112	TRIGout1	10.152	VCC107	VCC107.192	USB_FD_10	10.232
GND+	CLK2.33	VDLout1	10.73	led_2	10.113	CONF_DONE	CONF_DONE.153	GND	GND.193	USB_FD_6	10.233
USB_CLKOUT	CLK3.34	VCCINT	VCCINT.74	Ext_Trg_In	10.114	VCC106	VCC106.154	USB_PA_1	10.194	USB_PA_6	10.234
VCC102	VCC102.35	GND	GND.75	VCCINT	VCCINT.115	MSEL0	MSEL0.155	USB_PA_1	10.195	USB_PA_6	10.235
GND	GND.36	TRIGout4	10.76	GND	GND.116	GND	GND.156	USB_PA_2	10.196	USB_PA_6	10.236
ADC_Aux_3	10.37	VCC103	VCC103.77	CSB_Aux	10.117	MSEL1	MSEL1.157	USB_PA_5	10.197	USB_WAKEUP	10.237
ADC_Aux_3n	10.38	TOKout4	10.78	SCLK_Aux	10.118	MSEL2	MSEL2.158	VCCINT	VCCINT.198	USB_CTL_1	10.238
GND*	10.39	GND	GND.79	PDWN_Aux	10.119	RDClk	10.159	GND	GND.199	USB_FD_9	10.239
VCCINT	VCCINT.40	TRIGout2	10.80	SDIO_Aux	10.120	TRIGdelay_out2	10.160	USB_FD_1	10.200	led_0	10.240



**JTAG Connector**



Engineer	M. Bogdan	The University of Chicago	
Drawn by	M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637	
R&D CHK		TITLE	Siz
DATE:	8/16/2010	PSEC2 Flip Chip ADC Module	
TIME:	2:00 pm	FPGA	
UA CHK		REV	DRW. 2707
		Sheet 5 of 7	