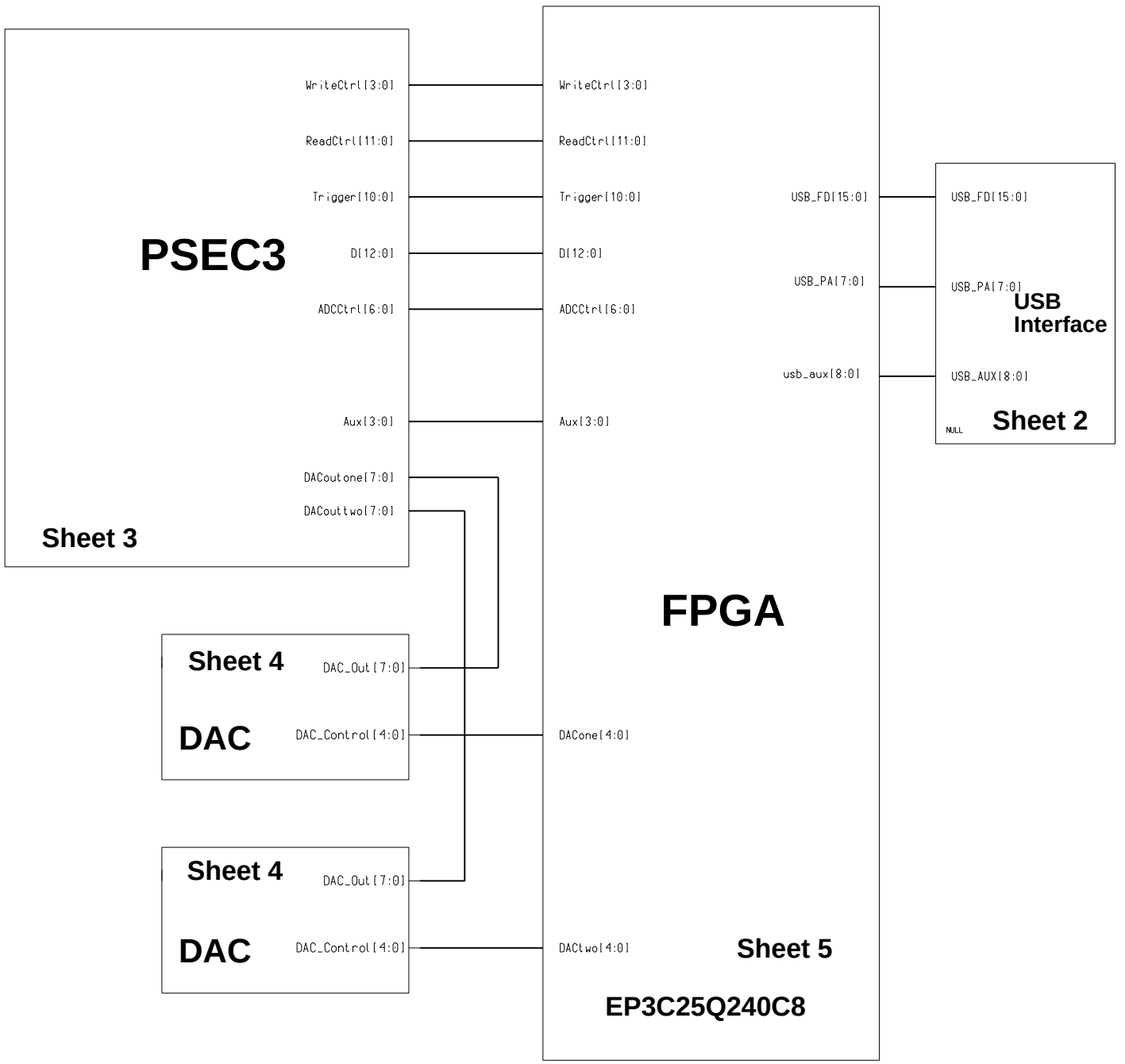
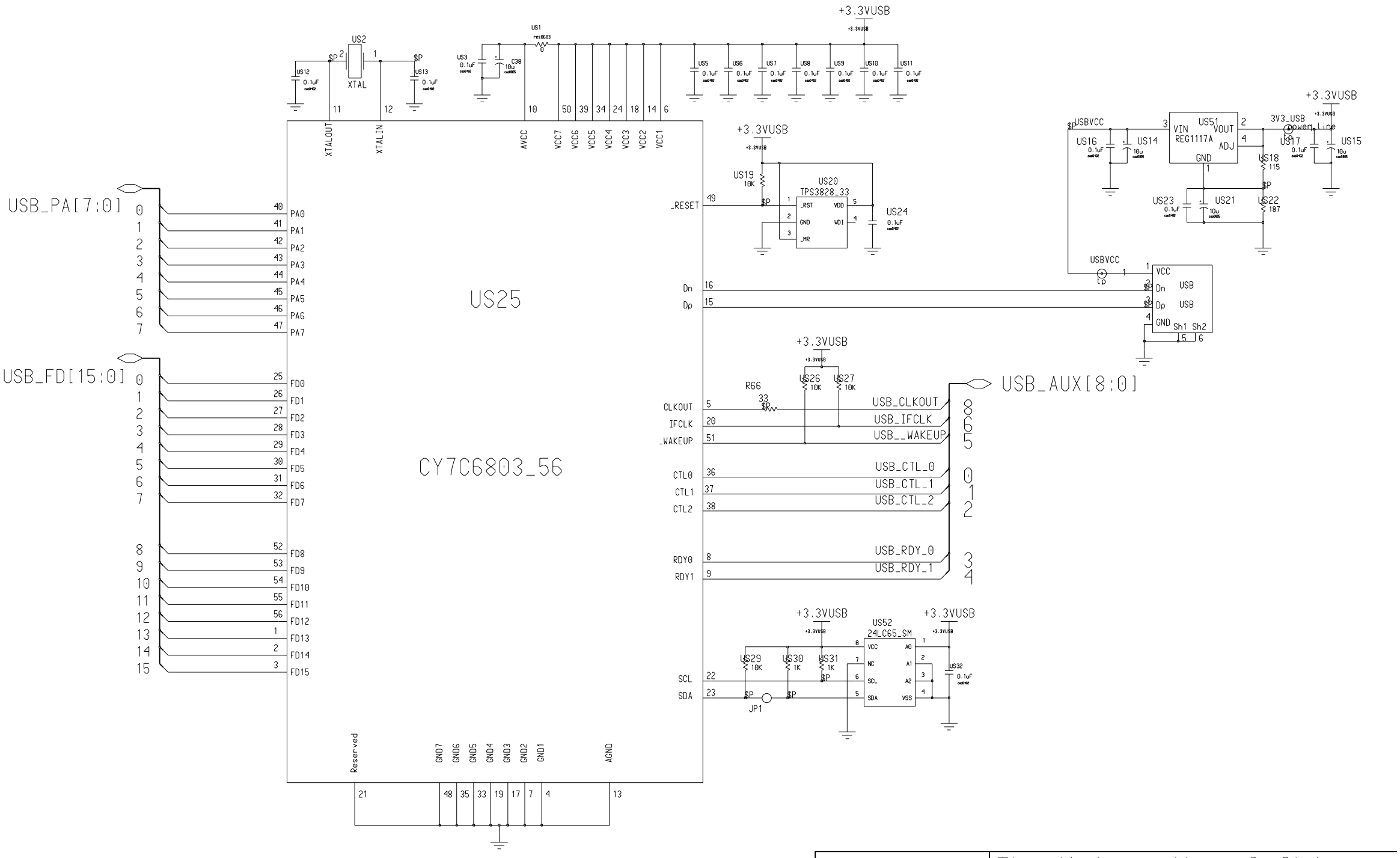


Engineer: M. Bogdan	**The University of Chicago**	
Drawn by: M. Bogdan	5640 S. Ellis Ave. Chicago, IL 60637	
DATE: 10/12/1010	Top Level	*PSEC3 Tester Module*
	REV. A | DRW. 2710	Sheet 1 of 5



Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637
Drawn by M.Bogdan	
R&D CHK	TITLE USB Interface *PSEC3 Tester Module*
DATE: 10/12/2010	Size B
TIME: 2:00 pm	
QA CHK	REV A | DRW. 2710 | Sheet 2 of 5

GND	1	CAV1	
GND	2	CAV2	
DAC_5	3	v2Gn	
TOKdecode_0	4	TOKdecodeX	
TOKdecode_1	5	TOKdecodeY	
TOKdecode_2	6	TOKdecodeZ	
+1.2Va	7	dvdd1	SP Power_17e
COMPtest_out	8	COMPtest_out	
DAC_6	9	COMPtest_in	
RO_mon	10	RO_mon	
sDAT_test	11	sDAT_test	
TOKout_2	12	TOKout_2	
TOKin_2	13	TOKin_2	
RDclk_2	14	ReadCLK_2	
GND	15	dgnd1	
16_TRIGbias	16	TRIGbias	SP
RAMP	17	RAMP	
18_RAMPbias	18	RAMPbias	SP
19_CEXT	19	CEXT	
20_RAMPbuffer_out	20	RAMPbuffer_out	SP
+1.2Va	21	avdd1	
DAC_7	22	DLLbias_1	
DAC_8	23	DLLbias_2	
24_DLL_Ipol_1	24	DLL_Ipol_1	SP
25_DLL_Iplo_2	25	DLL_Ipol_2	SP
GND	26	agnd1	
DLLreset	27	DLLreset	
DAToverflow	28	DAToverflow	
GND	29	dgnd2	
D_11	30	DAT_11	
D_10	31	DAT_10	
D_9	32	DAT_9	
D_8	33	DAT_8	
GND	34	dgnd3	
TRIGGER_5	35	TRIGGER_5	
D_7	36	DAT_7	
D_6	37	DAT_6	
D_5	38	DAT_5	
+1.2Va	39	dvdd2	
GND	40	dgnd4	
TRIGGER_4	41	TRIGGER_4	
TRIGGER_3	42	TRIGGER_3	
+1.2Va	43	dvdd3	
44_VCPout	44	VCPout	
DAC_10	45	VCPin	
copyMclk	46	copyMclk	
Dlout	47	DIout	
DAC_11	48	VCNin	
49_VCNout	49	VCNout	
+1.2Va	50	dvdd4	
TRIGGER_2	51	TRIGGER_2	
TRIGGER_1	52	TRIGGER_1	
TRIGGER_0	53	TRIGGER_0	
GND	54	dgnd5	
+1.2Va	55	dvdd5	
D_4	56	DAT_4	
D_3	57	DAT_3	
D_2	58	DAT_2	
D_1	59	DAT_1	
D_0	60	DAT_0	
GND	61	CAV3	
COMPbypass_sel	62	COMPbypass_sel	
ADClatch_ext	63	ADClatch_ext	
GND	64	dgnd6	
trig_EXT	65	trig_EXT	
trig_OR	66	trig_OR	
trig_EN	67	trig_EN	
trig_CLEAR	68	trig_CLEAR	
trig_SIGN	69	trig_SIGN	
+1.2Va	70	dvdd6	
Rdswitch_en	71	Rdswitch_en	
RO_en	72	RO_en	
clearADC	73	clearADC	
freq_sel	74	RO_freq_sel	
GND	75	dgnd7	
RDclk_1	76	ReadCLK_1	
+1.2Va	77	dvdd7	
TOKin_1	78	TOKin_1	
TOKout_1	79	TOKout_1	
CHANdecode_2	80	CHANdecodeZ	
CHANdecode_1	81	CHANdecodeY	
CHANdecode_0	82	CHANdecodeX	
+1.2Va	83	dvdd8	
DAC_12	84	thresh_5	
DAC_13	85	thresh_4	
DAC_14	86	thresh_3	
DAC_15	87	thresh_2	
DAC_16	88	thresh_1	
+1.2Va	89	avdd2	
GND	90	CAV4	
91_Analog_out	91	Analog_out	
DAC_1	92	vbias_0	
signal_0	93	signal_0	
GND	94	agnd2	
DAC_1	95	vbias_1	
signal_1	96	signal_1	
GND	97	agnd3	
+1.2Va	98	avdd3	
GND	99	agnd4	
DAC_1	100	vbias_2	
signal_2	101	signal_2	
GND	102	dgnd_8	
Mclk	103	Mclk	
+1.2Va	104	dvdd9	
signal_3	105	signal_3	
DAC_1	106	vbias_3	
GND	107	agnd_5	
+1.2Va	108	avdd_4	
GND	109	agnd_6	
signal_4	110	signal_4	
DAC_1	111	vbias_4	
+1.2Va	112	dvdd10	
+1.2Va	113	avdd5	
GND	114	agnd7	
signal_5	115	signal_5	
DAC_1	116	vbias_5	
Rofan_mon	117	Rofan_mon	
DAC_2	118	VswP	
DAC_3	119	VswN	
DAC_4	120	v2Gp	

WriteCtrl[3:0]
- 0 — Mclk
- 1 — copyMclk
- 2 — DLLreset
- 3 — Dlout

ADCCtrl[6:0]
- 0 — Rdswitch_en
- 1 — RO_en
- 2 — clearADC
- 3 — freq_sel
- 4 — RO_mon
- 5 — Rofan_mon
- 6 — RAMP

ReadCtrl[11:0]
- 0 — TOKdecode_0
- 1 — TOKdecode_1
- 2 — TOKdecode_2
- 3 — TOKin_1
- 4 — TOKin_2
- 5 — RDclk_1
- 6 — RDclk_2
- 7 — CHANdecode_0
- 8 — CHANdecode_1
- 9 — CHANdecode_2
- 10 — TOKout_1
- 11 — TOKout_2

D[12:0]
- 0 — D_0
- 1 — D_1
- 2 — D_2
- 3 — D_3
- 4 — D_4
- 5 — D_5
- 6 — D_6
- 7 — D_7
- 8 — D_8
- 9 — D_9
- 10 — D_10
- 11 — D_11
- 12 — DAToverflow

Trigger[10:0]
- 0 — TRIGGER_0
- 1 — TRIGGER_1
- 2 — TRIGGER_2
- 3 — TRIGGER_3
- 4 — TRIGGER_4
- 5 — TRIGGER_5
- 6 — trig_EXT
- 7 — trig_EN
- 8 — trig_CLEAR
- 9 — trig_SIGN
- 10 — trig_OR

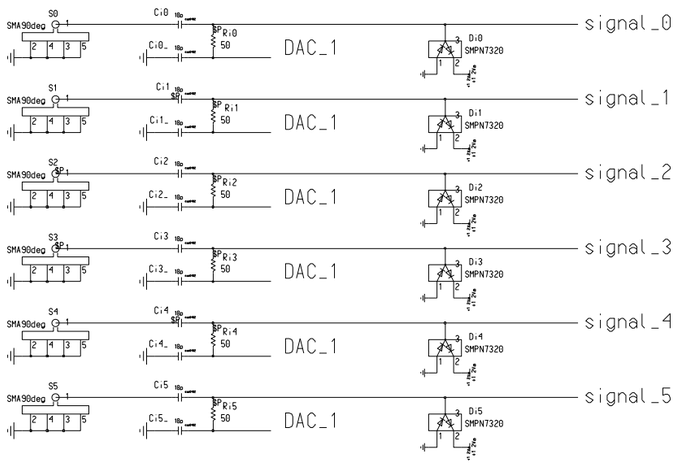
Aux[3:0]
- 0 — COMPbypass_sel
- 1 — ADClatch_ext
- 2 — COMPtest_out
- 3 — sDAT_test

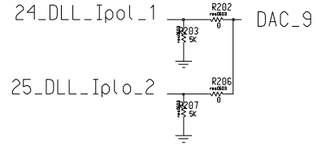
TP1 — SP 19_CEXT
TP2 — 20_RAMPbuffer_out
TP3 — SP 44_VCPout
TP4 — SP 49_VCNout
TP5 — SP 91_Analog_out

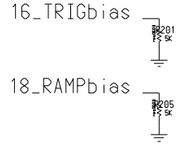
DACout one[7:0]
- 0 — DAC_1
- 1 — DAC_2
- 2 — DAC_3
- 3 — DAC_4
- 4 — DAC_5
- 5 — DAC_6
- 6 — DAC_7
- 7 — DAC_8

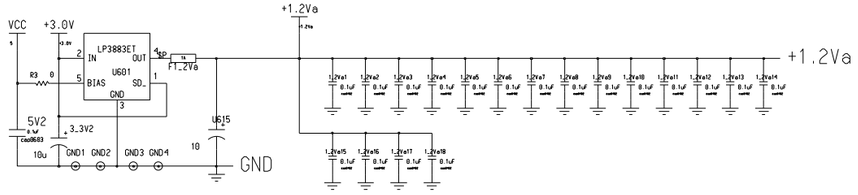
DACout two[7:0]
- 0 — DAC_9
- 1 — DAC_10
- 2 — DAC_11
- 3 — DAC_12
- 4 — DAC_13
- 5 — DAC_14
- 6 — DAC_15
- 7 — DAC_16

PSEC3
PSEC3





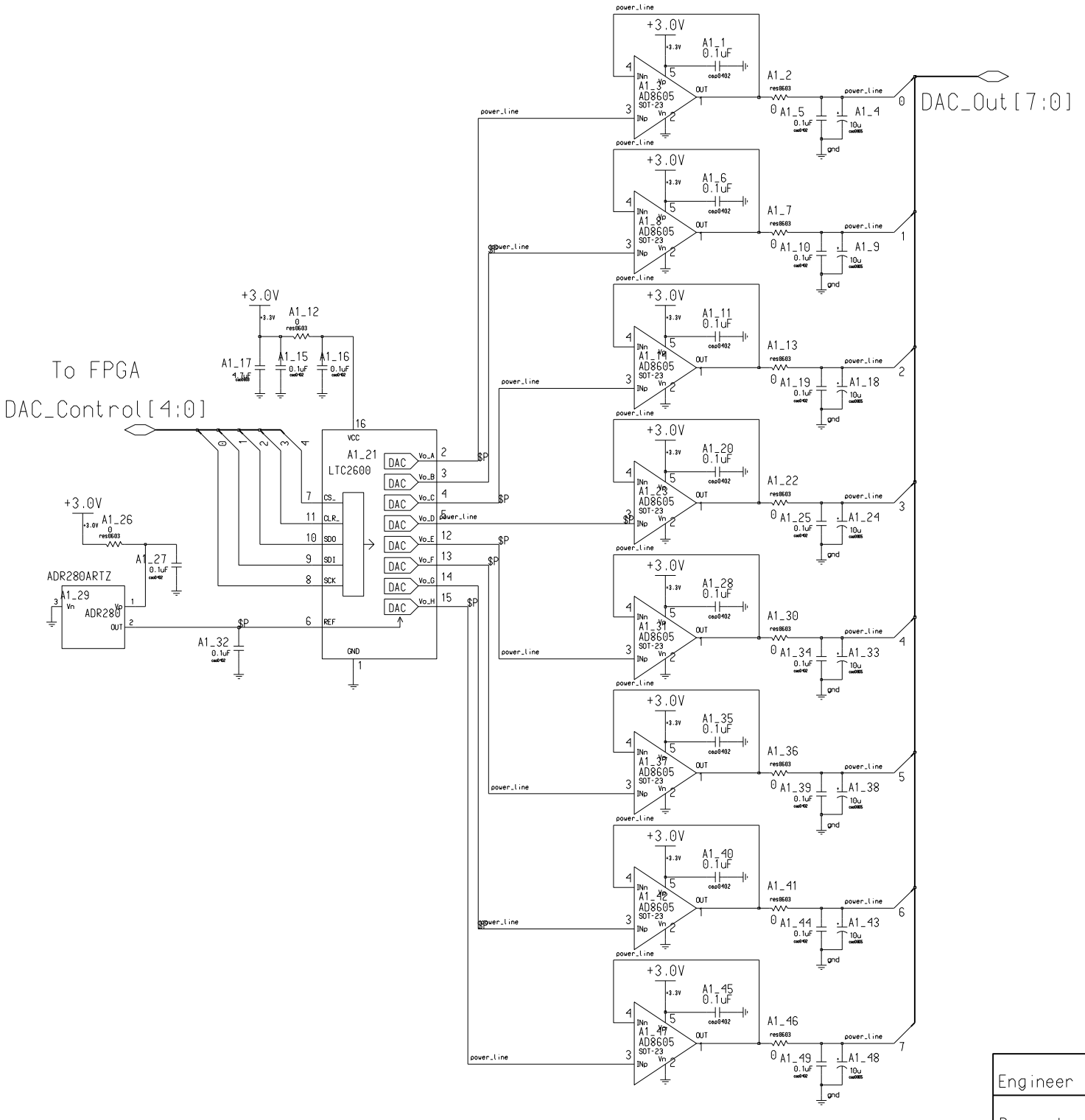




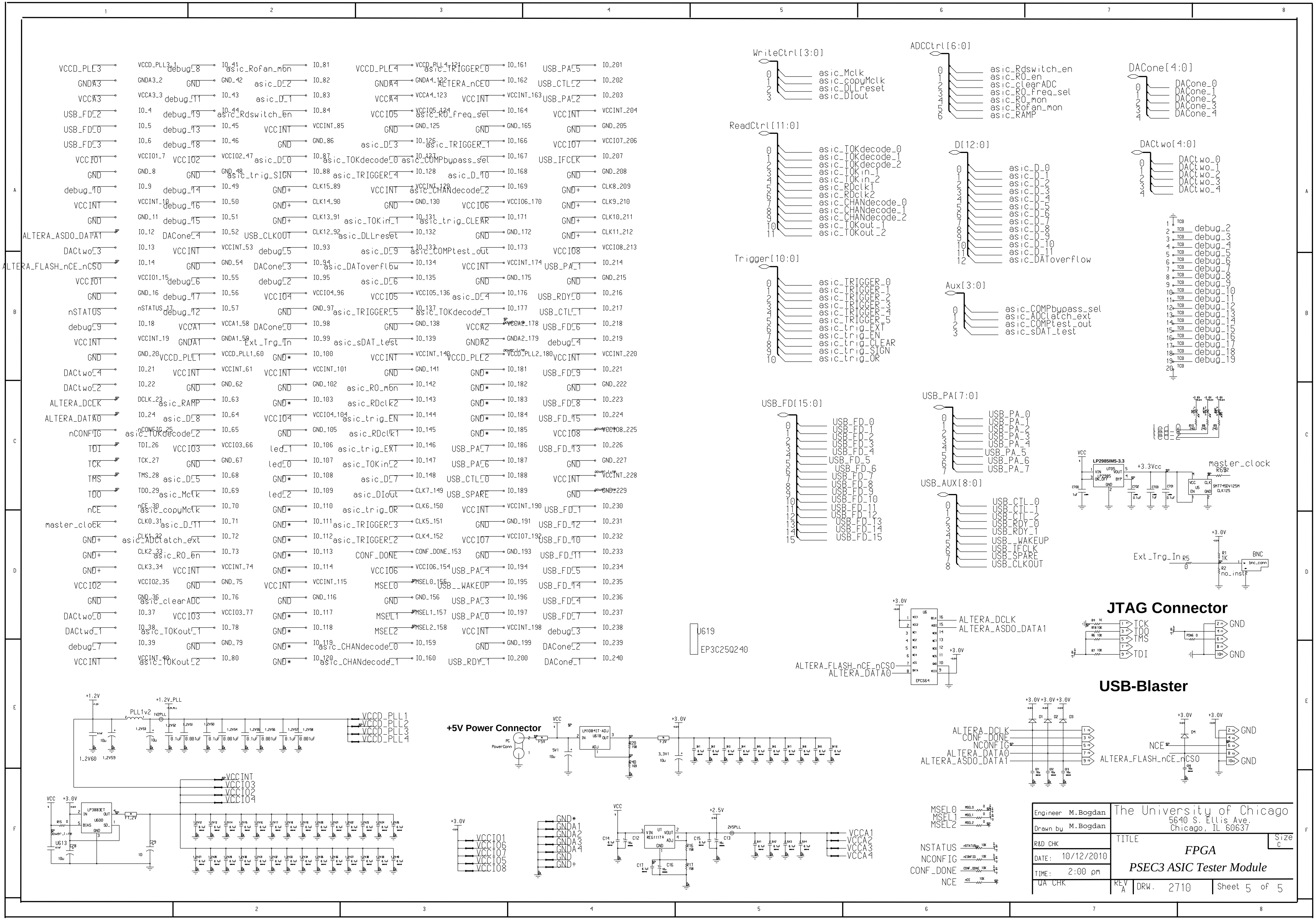
44_VCPout — R200 — DAC_10

49_VCNout — R204 — DAC_11

Engineer	M.Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637	
Drawn by	M.Bogdan		
R&D CHK		TITLE *PSEC3 - ASIC* *PSEC3 Tester Board*	Size C
DATE:	10/22/2010		
TIME:	2:00 pm		
QA CHK		REV A | DRW. 2710	Sheet 3 of 5



Engineer M.Bogdan	The University of Chicago 5640 S. Ellis Ave, Chicago, IL 60637
Drawn by M.Bogdan	
R&D CHK	*DAC* *PSEC3 Tester Module*
DATE: 10/12/2010	
TIME: 2:00 pm	
QA CHK	REV A / DRW. 2710 / Sheet 4/5


JTAG Connector
USB-Blaster
+5V Power Connector
WriteCtrl[3:0]
ADCCtrl[6:0]
DACone[4:0]
ReadCtrl[11:0]
D[12:0]
DACtwo[4:0]
Trigger[10:0]
Aux[3:0]
USB_FD[15:0]
USB_PA[7:0]
USB_AUX[8:0]
U619
EP3C25Q240
EPCS64
LP2985IM5-3.3
master_clock
Ext_Trg_In
BNC
Engineer M.Bogdan
Drawn by M.Bogdan
R&D CHK
DATE: 10/12/2010
TIME: 2:00 pm
QA CHK
The University of Chicago
5640 S. Ellis Ave.
Chicago, IL 60637
TITLE
FPGA
PSEC3 ASIC Tester Module
Size C
REV A
DRW. 2710
Sheet 5 of 5