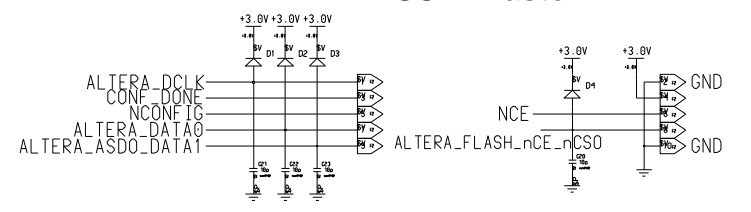
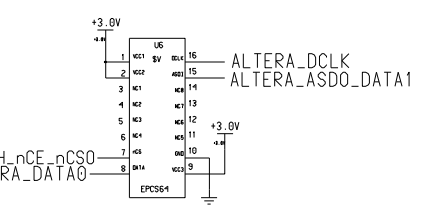
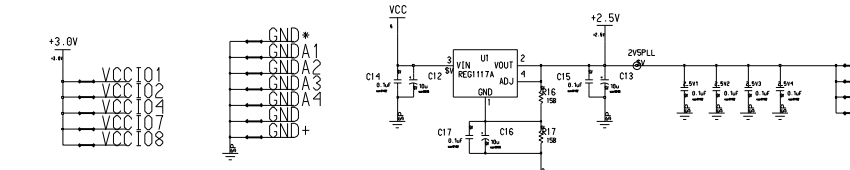
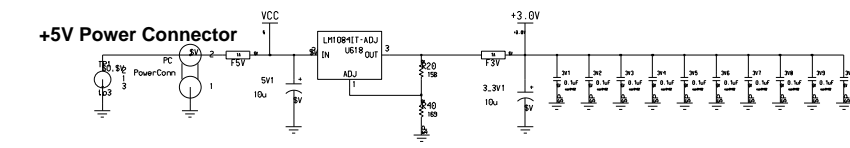
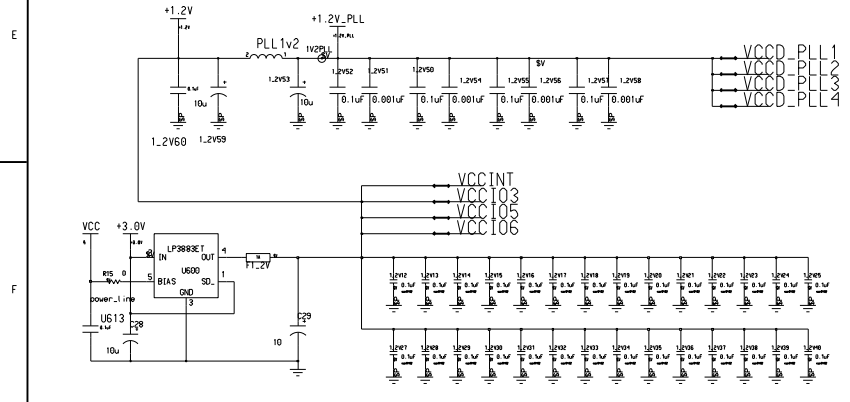
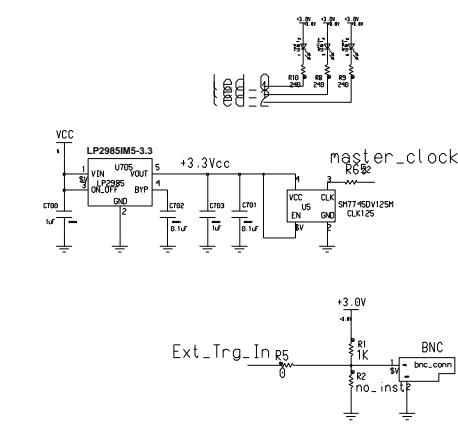
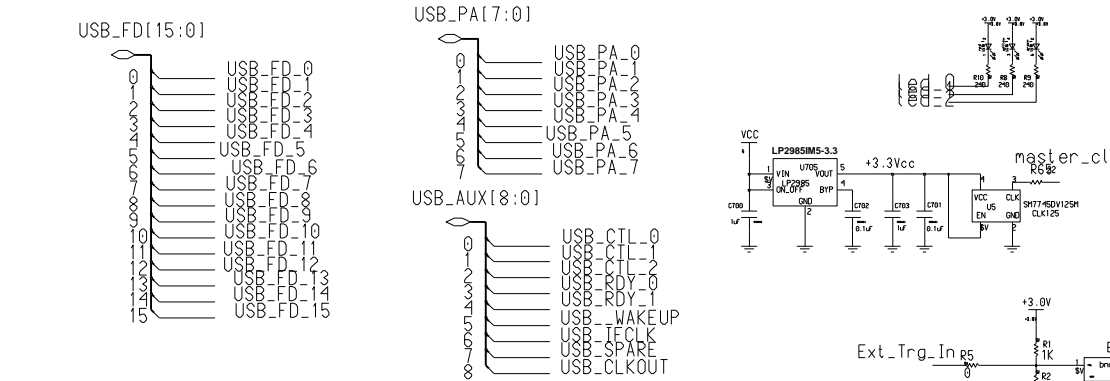
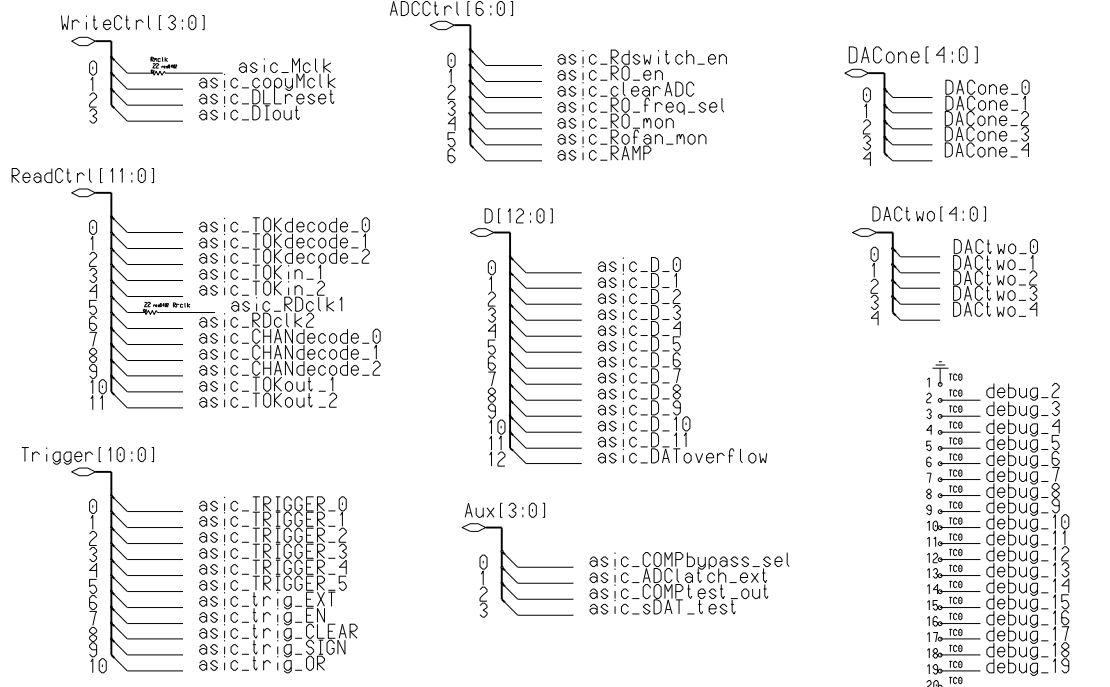


VCCD_PLL3	VCCD_PLL3_1	debug_18	10_41	asic_Rofan_mon	10_81	VCCD_PLL4	VCCD_PLL4_1	TRIGGER_0	10_161	USB_PA_5	10_201
GND_A3	GND_A3_2	GND	GND_42	asic_D_2	10_82	GND_A4	GND_A4_1	ALTERA_nCEO	10_162	USB_CTL_2	10_202
VCCA3	VCCA3_3	debug_11	10_43	asic_D_1	10_83	VCCA4	VCCA4_123	VCCINT_163	VCCINT_163	USB_PA_2	10_203
USB_FD_2	10_4	debug_19	10_44	asic_Rdswich_en	10_84	VCC105	VCC105_1	asic_RO_freq_sel	10_164	VCCINT	VCCINT_204
USB_FD_0	10_5	debug_13	10_45	VCCINT	VCCINT_85	GND	GND_125	GND	GND_165	GND	GND_205
USB_FD_3	10_6	debug_18	10_46	GND	GND_86	asic_D_3	10_126	asic_TRIGGER_1	10_166	VCC107	VCC107_206
VCC101	VCC101_7	VCC102	VCC102_47	asic_D_0	10_87	asic_TOKdecode_0	10_127	asic_COMPbypass_set	10_167	USB_IFCLK	10_207
GND	GND_8	GND	GND_48	asic_trig_SIGN	10_88	asic_TRIGGER_4	10_128	asic_D_10	10_168	GND	GND_208
debug_10	10_9	debug_14	10_49	GND	CLK15_89	VCCINT	VCCINT_129	asic_CHANdecode_2	10_169	GND	CLK8_209
VCCINT	VCCINT_10	debug_16	10_50	GND	CLK14_90	GND	GND_130	VCC106	VCC106_170	GND	CLK9_210
GND	GND_11	debug_15	10_51	GND	CLK13_91	asic_TOKin_1	10_131	asic_trig_CLEAR	10_171	GND	CLK10_211
ALTERA_ASDO_DATA1	10_12	DAConE_4	10_52	USB_CLKOUT	CLK12_92	asic_DLLreset	10_132	GND	GND_172	GND	CLK11_212
DACTwo_3	10_13	VCCINT	VCCINT_53	debug_5	10_93	asic_D_9	10_133	asic_COMPTest_out	10_173	VCC108	VCC108_213
ALTERA_FLASH_nCE_nCS0	10_14	GND	GND_54	DAConE_3	10_94	asic_DATAoverflow	10_134	VCCINT	VCCINT_174	USB_PA_1	10_214
VCC101	VCC101_15	debug_6	10_55	debug_2	10_95	asic_D_6	10_135	GND	GND_175	GND	GND_215
GND	GND_16	debug_17	10_56	VCC104	VCC104_96	VCC105	VCC105_136	asic_D_4	10_176	USB_RDY_0	10_216
nSTATUS	nSTATUS_1	debug_12	10_57	GND	GND_97	asic_TRIGGER_5	10_177	asic_TOKdecode_1	10_177	USB_CTL_1	10_217
debug_9	10_18	VCCA1	VCCA1_58	DAConE_0	10_98	GND	GND_138	VCCA2	VCCA2_178	USB_FD_6	10_218
VCCINT	VCCINT_19	GNDAT	GNDAT_59	Ext_Trg_In	10_99	asic_sDAT_test	10_139	GND_A2	GND_A2_179	debug_4	10_219
GND	GND_20	VCCD_PLL1	VCCD_PLL1_60	GND	10_100	VCCINT	VCCINT_140	VCCD_PLL2	VCCD_PLL2_180	VCCINT	VCCINT_220
DACTwo_4	10_21	VCCINT	VCCINT_61	VCCINT	10_101	GND	GND_141	GND	GND_181	USB_FD_9	10_221
DACTwo_2	10_22	GND	GND_62	GND	GND_102	asic_RO_mon	10_142	GND	GND_182	GND	GND_222
ALTERA_DCLK	DCLK_23	asic_RAMP	10_63	GND	10_103	asic_RDclk_2	10_143	GND	10_183	USB_FD_8	10_223
ALTERA_DATA0	10_24	asic_D_8	10_64	VCC104	VCC104_104	asic_trig_EN	10_144	GND	10_184	USB_FD_15	10_224
nCONF_16	10_25	asic_TOKdecode_2	10_65	GND	GND_105	asic_RDclk_1	10_145	GND	10_185	VCC108	VCC108_225
TDI	TDI_26	VCC103	VCC103_66	led_1	10_106	asic_trig_EXT	10_146	USB_PA_7	10_186	USB_FD_3	10_226
TCK	TCK_27	GND	GND_67	led_0	10_107	asic_TOKin_2	10_147	USB_PA_6	10_187	GND	GND_227
TMS	TMS_28	asic_D_5	10_68	GND	10_108	asic_D_7	10_148	USB_CTL_0	10_188	VCCINT	VCCINT_228
TDO	TDO_29	asic_Mclk	10_69	led_2	10_109	asic_DIOut	CLK7_149	USB_SPARE	10_189	GND	GND_229
nCE	nCE_30	asic_copyMclk	10_70	GND	10_110	asic_trig_OR	CLK6_150	VCCINT	VCCINT_190	USB_FD_1	10_230
master_clock	CLK0_31	asic_D_11	10_71	GND	10_111	asic_TRIGGER_3	CLK5_151	GND	GND_191	USB_FD_12	10_231
GND	GND_32	asic_ADClatch_ext	10_72	GND	10_112	asic_TRIGGER_2	CLK4_152	VCC107	VCC107_192	USB_FD_10	10_232
GND	GND_33	asic_RO_en	10_73	GND	10_113	CONF_DONE	CONF_DONE_153	GND	GND_193	USB_FD_11	10_233
GND	GND_34	VCCINT	VCCINT_74	GND	10_114	VCC106	VCC106_154	USB_PA_4	10_194	USB_FD_5	10_234
VCC102	VCC102_35	GND	GND_75	VCCINT	VCCINT_115	MSEL0	MSEL0_155	USB_WAKEUP	10_195	USB_FD_14	10_235
GND	GND_36	asic_clearADC	10_76	GND	GND_116	GND	GND_156	USB_PA_3	10_196	USB_FD_4	10_236
DACTwo_0	10_37	VCC103	VCC103_77	GND	10_117	MSEL1	MSEL1_157	USB_PA_0	10_197	USB_FD_7	10_237
DACTwo_1	10_38	asic_TOKout_1	10_78	GND	10_118	MSEL2	MSEL2_158	VCCINT	VCCINT_198	debug_3	10_238
debug_7	10_39	GND	GND_79	GND	10_119	asic_CHANdecode_0	10_159	GND	GND_199	DAConE_2	10_239
VCCINT	VCCINT_40	asic_TOKout_2	10_80	GND	10_120	asic_CHANdecode_1	10_160	USB_RDY_1	10_200	DAConE_1	10_240



Engineer	M. Bogdan	The University of Chicago	
Drawn by	M. Bogdan	5640 S. Ellis Ave.	
R&D CHK		Chicago, IL 60637	
DATE:	2/22/2011	TITLE	FPGA
TIME:	11:17 am	PSEC3 ASIC Tester Module	
UA CHK	REV B	DRW.	2710
			Sheet 5 of 5