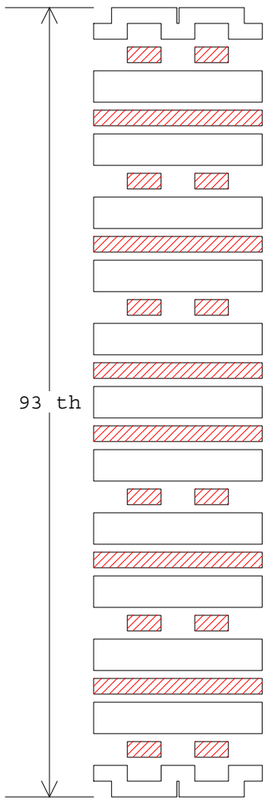
Layer Stackup. Design: psec_cc, Designer: bogdan.

Number of layers: ~~25~~
Total thickness = 93 th



NN	Layer Name	Type	Usage	Thickness th	Er	Z0 ohm
1	DIELECTRIC_1	Dielectric	Solder Mask	1	1	
2	SIGNAL_1	Metal	Signal	1.4	1	53.7
3	DIELECTRIC_3	Dielectric	Substrate	3.5	4.4	
4	Plane1	Metal	Solid Plane	1.4	1	
5	DIELECTRIC_5	Dielectric	Substrate	7	4.4	
6	SIGNAL_2	Metal	Signal	0.7	1	53.8
7	DIELECTRIC_7	Dielectric	Substrate	7	4.4	
8	Plane2	Metal	Solid Plane	1.4	1	
9	DIELECTRIC_9	Dielectric	Substrate	7	4.4	
10	SIGNAL_3	Metal	Signal	0.7	1	53.8
11	DIELECTRIC_11	Dielectric	Substrate	7	4.4	
12	Plane3	Metal	Solid Plane	1.4	1	
13	DIELECTRIC_13	Dielectric	Substrate	14	4.4	
14	Plane4	Metal	Solid Plane	1.4	1	
15	DIELECTRIC_15	Dielectric	Substrate	7	4.4	
16	SIGNAL_4	Metal	Signal	0.7	1	53.8
17	DIELECTRIC_17	Dielectric	Substrate	7	4.4	
18	Plane5	Metal	Solid Plane	1.4	1	
19	DIELECTRIC_19	Dielectric	Substrate	7	4.4	
20	SIGNAL_5	Metal	Signal	0.7	1	53.8
21	DIELECTRIC_21	Dielectric	Substrate	7	4.4	
22	Plane6	Metal	Solid Plane	1.4	1	
23	DIELECTRIC_23	Dielectric	Substrate	3.5	4.4	
24	SIGNAL_6	Metal	Signal	1.4	1	53.7
25	DIELECTRIC_25	Dielectric	Solder Mask	1	1	

The University of Chicago
Electronics Design Group

01/06/12

PSEC DAQ CC

Specification Drawing # 2767

Notes:
1. Number of Layers: 12;
2. Board Size: 6"x6";
3. Material FR4 with Tg >170C;
4. 1 Oz Copper for all planes and for Top and Bottom;
5. 1/2 Oz Copper for all Stripline Trace Layers;
6. Immersion Gold plating with min Ni: 2.5-5um; Au: 0.05-0.2um;
7. Board Thickness: 93 mil +/- 10%;
8. Silkscreen on both sides;
9. FHS tolerance: +/- 3 mil;
10. Minimum trace width/clearance: 5 mil;
11. Impedance Control: Zc=50 Ohm for all 5 mil traces;