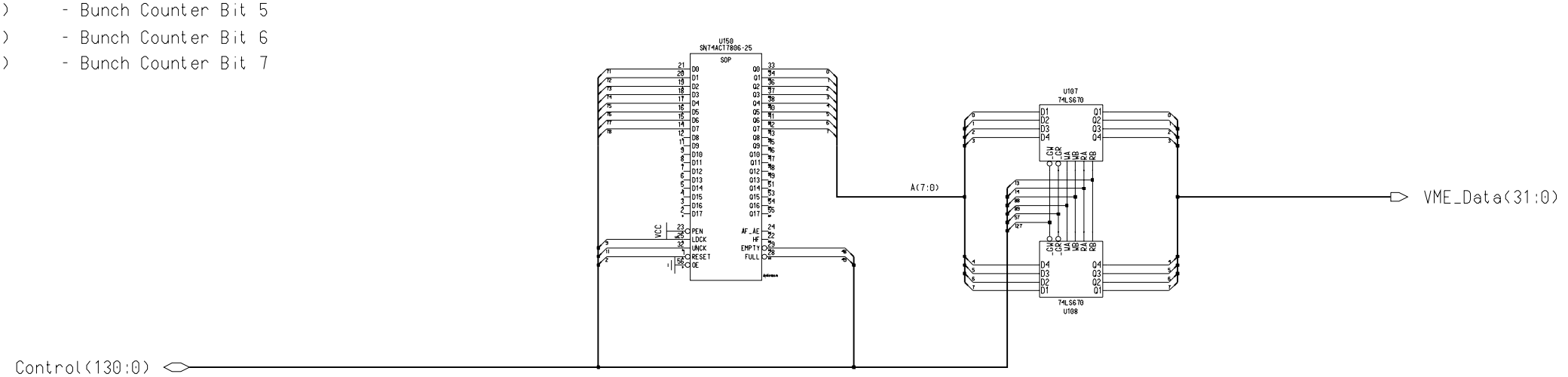
Bunch_Counter

Control Signals

Control(2) - Reset*
Control(9) - Write Bunch Counter Clock
Control(11) - Read Clock
Control(48) - Bunch Counter FIFO Empty flag*
Control(49) - Bunch Counter FIFO Full flag*
Control(13) - Read Address B (Set 1)
Control(14) - Read Address A (Set 1)
Control(88) - Write Address B (Set 1)
Control(89) - Write Address A (Set 1)
Control(127) - Buffer Write Enable* (1)
Control(57) - Bunch Counter Buffer Read Enable*
Control(71) - Bunch Counter Bit 0
Control(72) - Bunch Counter Bit 1
Control(73) - Bunch Counter Bit 2
Control(74) - Bunch Counter Bit 3
Control(75) - Bunch Counter Bit 4
Control(76) - Bunch Counter Bit 5
Control(77) - Bunch Counter Bit 6
Control(78) - Bunch Counter Bit 7



DATE	REVISION DESCRIPTION
4 Oct 98	Changed to TI SN74ACT7806 FIFO chip. --NJL
29 Oct 98	Buffers: read addresses, write addresses, and write enables changed to driver outputs. -NJL

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Bunch_Counter

SHEET 14 OF 20
DATE 27 Aug 98
DRWN Nancy J. Lai

C-2329
REV A