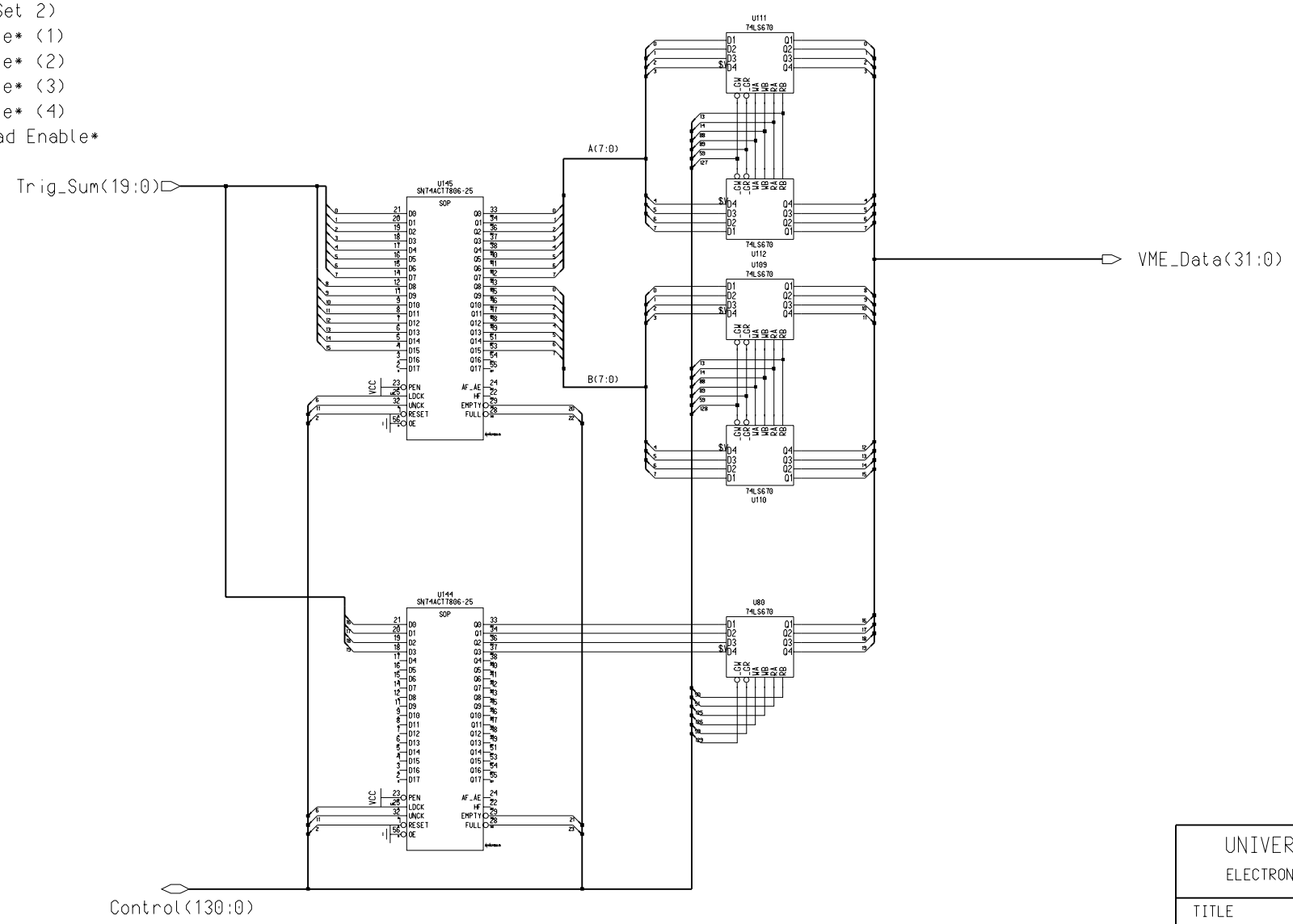
Trig_Sum_DAQ

Control Signals

Control(2) - Reset*
Control(6) - Write Trig_Sum Clock
Control(11) - Read Clock
Control(20) - Trig_Sum FIFO1 Empty flag*
Control(21) - Trig_Sum FIFO2 Empty flag*
Control(22) - Trig_Sum FIFO1 Full flag*
Control(23) - Trig_Sum FIFO2 Full flag*
Control(13) - Read Address B (Set 1)
Control(14) - Read Address A (Set 1)
Control(50) - Read Address B (Set 2)
Control(51) - Read Address A (Set 2)
Control(88) - Write Address B (Set 1)
Control(89) - Write Address A (Set 1)
Control(125) - Write Address B (Set 2)
Control(126) - Write Address A (Set 2)
Control(127) - Buffer Write Enable* (1)
Control(128) - Buffer Write Enable* (2)
Control(129) - Buffer Write Enable* (3)
Control(130) - Buffer Write Enable* (4)
Control(59) - Trig_Sum Buffer Read Enable*



DATE	REVISION DESCRIPTION
4 Oct 98	Changed to TI SN74ACT7806 FIFO chip. --NJL
29 Oct 98	Buffers: read addresses, write addresses, and write enables changed to driver outputs. -NJL

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Crate Sum/TRIG_Sum_DAQ

SHEET 16 OF 20
DATE 2 July 98
DRWN Nancy J. Lai

C-2329
REV A