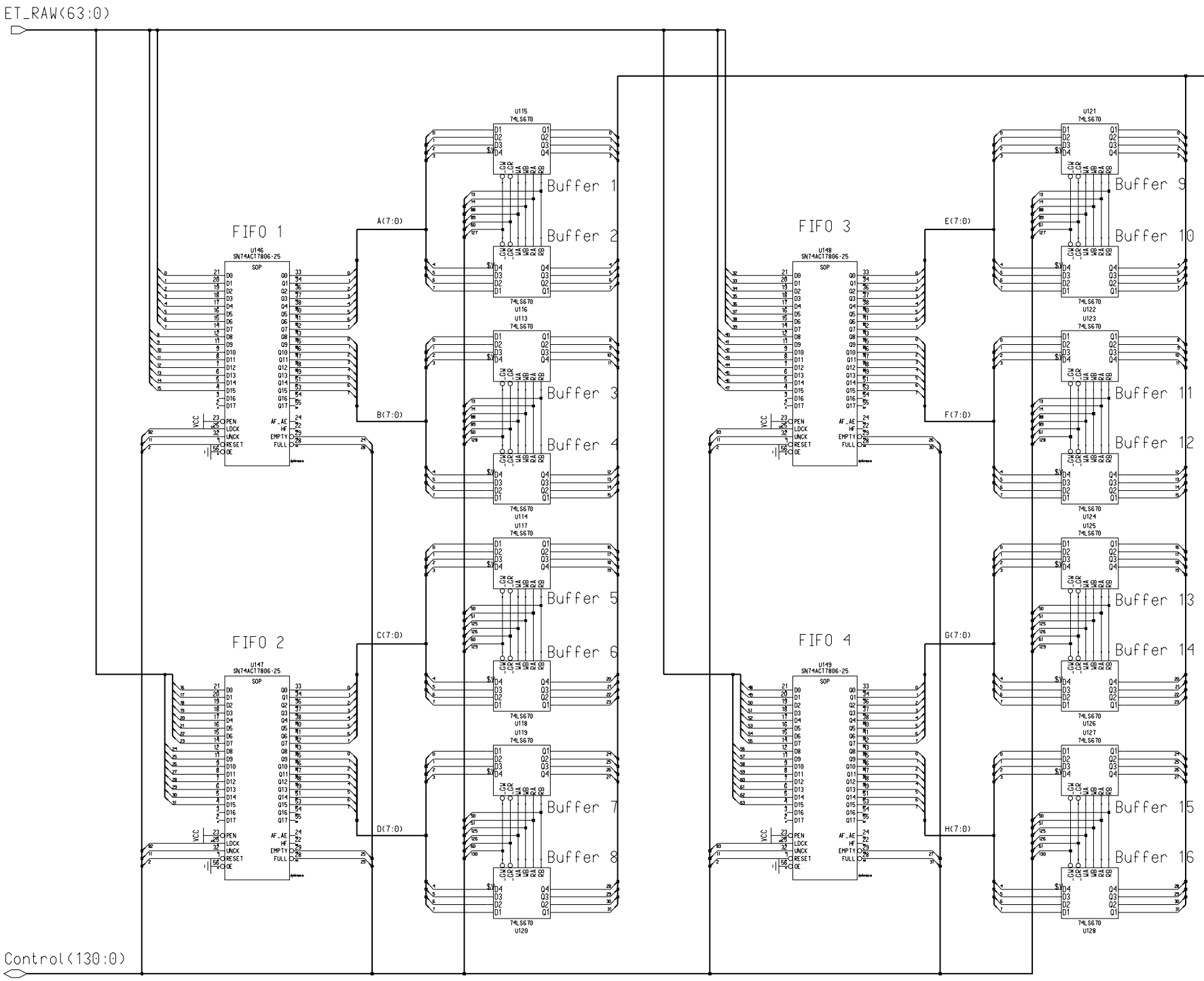
ET_RAW_DAQ



Control Signals

Control(2)	- Reset*
Control(11)	- Read Clock
Control(24)	- ET_RAW FIFO1 Empty flag*
Control(25)	- ET_RAW FIFO2 Empty flag*
Control(26)	- ET_RAW FIFO3 Empty flag*
Control(27)	- ET_RAW FIFO4 Empty flag*
Control(28)	- ET_RAW FIFO1 Full flag*
Control(29)	- ET_RAW FIFO2 Full flag*
Control(30)	- ET_RAW FIFO3 Full flag*
Control(31)	- ET_RAW FIFO4 Full flag*
Control(13)	- Read Address B (Set 1)
Control(14)	- Read Address A (Set 1)
Control(50)	- Read Address B (Set 2)
Control(51)	- Read Address A (Set 2)
Control(88)	- Write Address B (Set 1)
Control(89)	- Write Address A (Set 1)
Control(125)	- Write Address B (Set 2)
Control(126)	- Write Address A (Set 2)
Control(127)	- Buffer Write Enable* (1)
Control(128)	- Buffer Write Enable* (2)
Control(129)	- Buffer Write Enable* (3)
Control(130)	- Buffer Write Enable* (4)
Control(60)	- ET_RAW Buffers 1-8 Read Enable*
Control(61)	- ET_RAW Buffers 9-16 Read Enable*
Control(82)	- Write ET_RAW Wedge 0 Clock
Control(83)	- Write ET_RAW Wedge 1 Clock

DATE	REVISION DESCRIPTION
4 Oct 98	Changed to TI SN74ACT7806 FIFO chip. --NJL
29 Oct 98	Buffers: read addresses, write addresses, and write enables changed to driver outputs. -NJL

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Crate Sum/ET_RAW_DAQ

SHEET 17 OF 20
DATE 2 July 98
DRWN Nancy J. Lai

C-2329
REV A