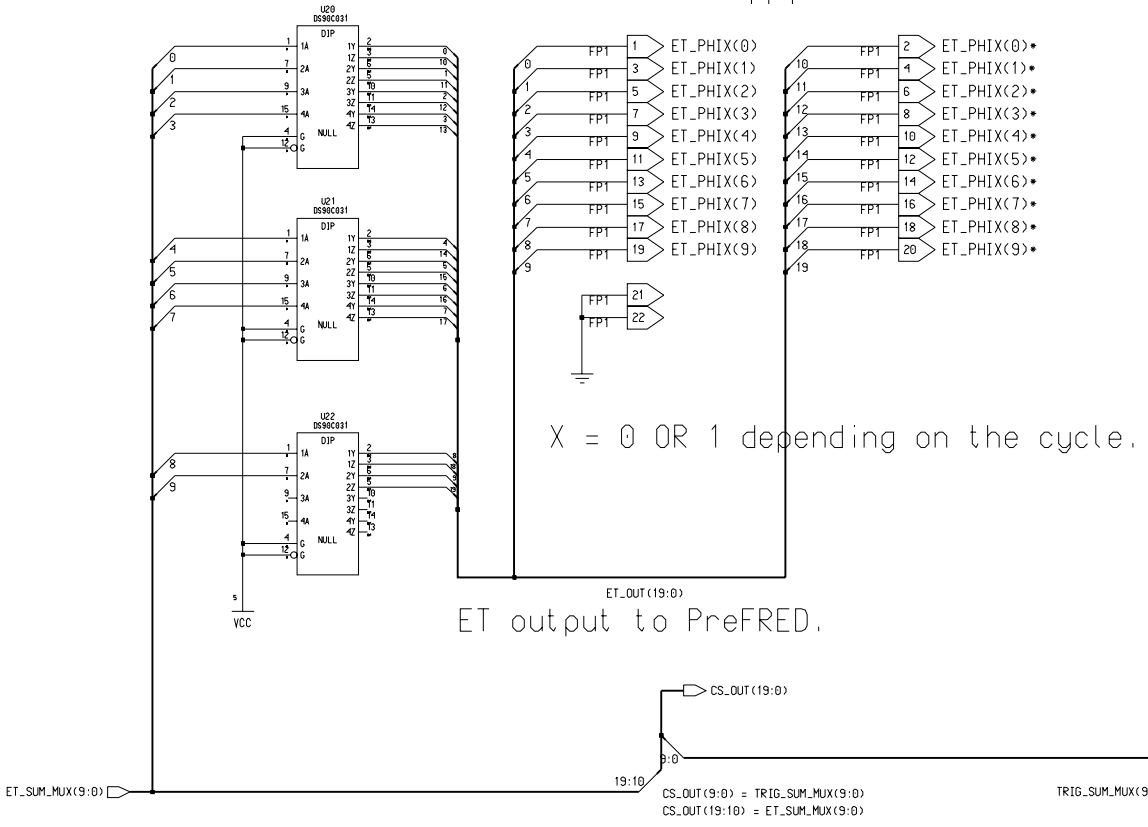


Differential Drivers

FP1

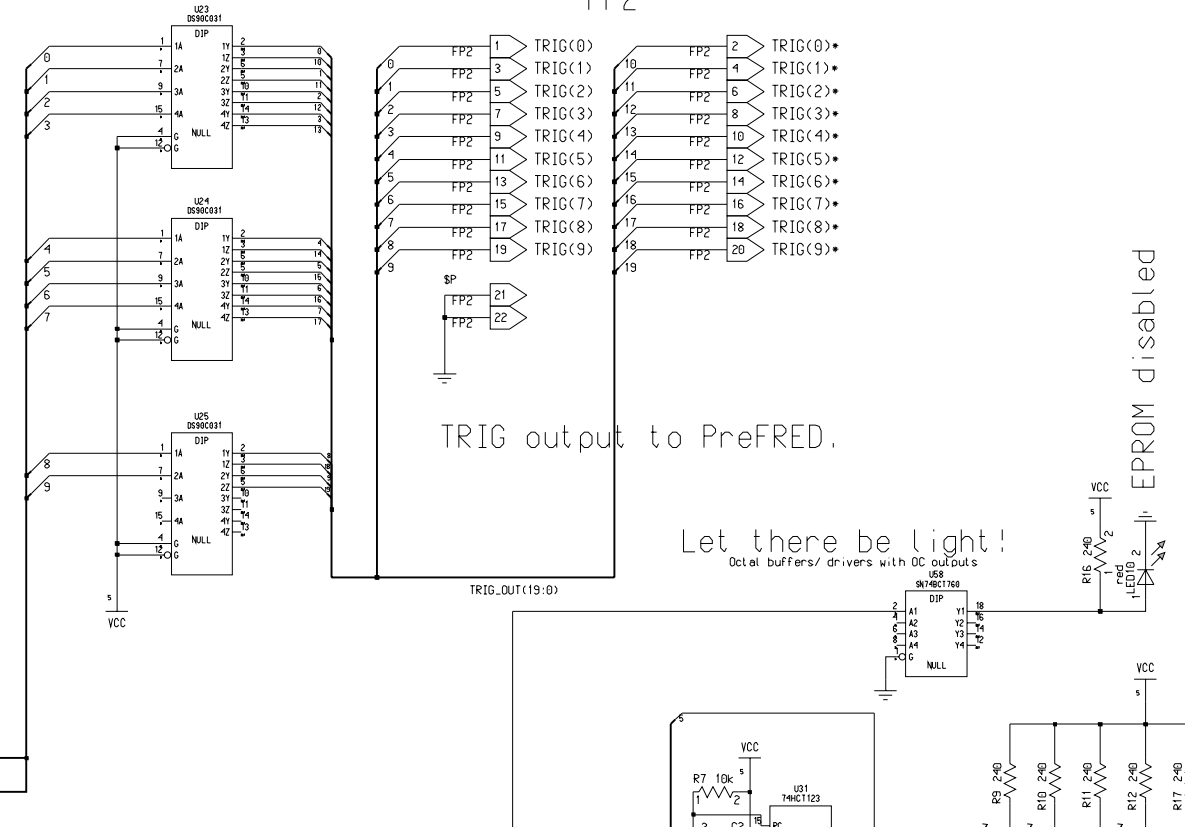
Differential Drivers

FP2



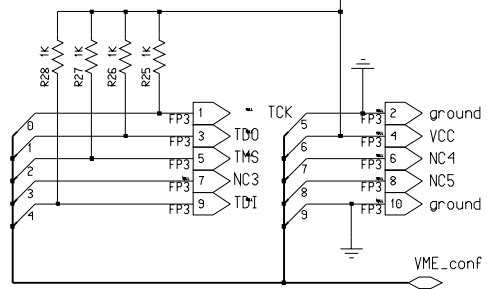
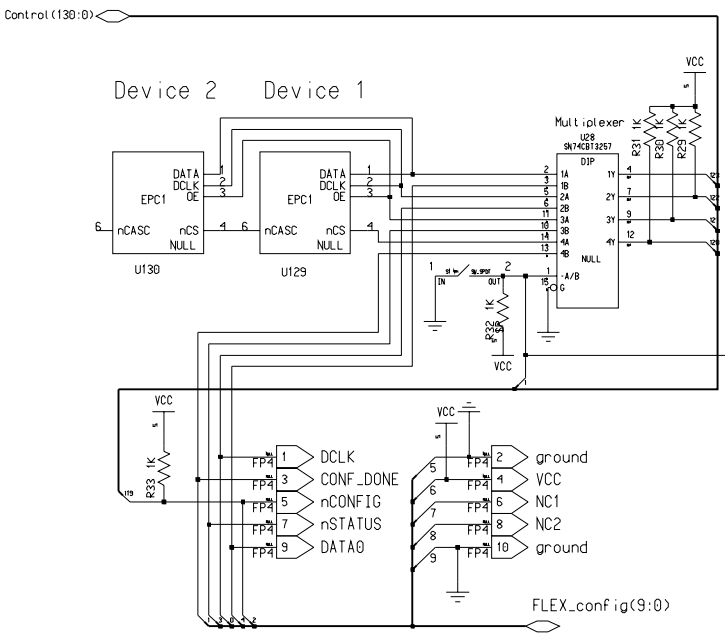
X = 0 OR 1 depending on the cycle.

ET output to PrefRED.



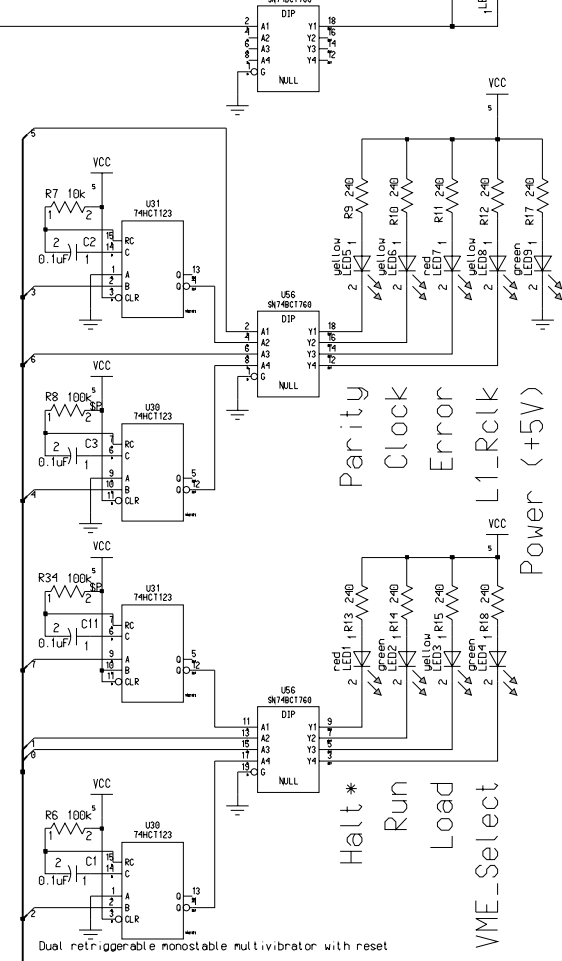
TRIG output to PrefRED.

Let there be light!
Octal buffers/drivers with OC outputs



FP3: connector to VME-Interface Bit Blaster (JTAG mode)

FP4: connector to Bit Blaster Download Cable (PS mode)



The parity LED lights up when the even wedge ET summary is sent first.
Note that these signals are multiplexed in two sequential steps of 66 ns each.

Lights<7:0>

DATE	REVISION DESCRIPTION
6 Mar 98	Made everything consistent with 10 lines of ET_OUT and TRIG_OUT. -NJL
8/15/98	put new symbols
31 Aug 98	Updated Lights signals. -NJL
May 28 99	Added monostabil on Lights<7>

UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP	
TITLE Crate Sum/FP	
SHEET 19 OF 20	C-2329
DATE 16 May 96	REV A
DRWN Dave Toback	