Differential Drivers

FP1

U20 DS90C031 DIP
U21 DS90C031 DIP
U22 DS90C031 DIP
1A 2A 3A 4A G G NULL
1Y 1Z 2Y 2Z 3Y 3Z 4Y 4Z

FP1 ET_PHIX(0) ET_PHIX(0)*
FP1 ET_PHIX(1) ET_PHIX(1)*
FP1 ET_PHIX(2) ET_PHIX(2)*
FP1 ET_PHIX(3) ET_PHIX(3)*
FP1 ET_PHIX(4) ET_PHIX(4)*
FP1 ET_PHIX(5) ET_PHIX(5)*
FP1 ET_PHIX(6) ET_PHIX(6)*
FP1 ET_PHIX(7) ET_PHIX(7)*
FP1 ET_PHIX(8) ET_PHIX(8)*
FP1 ET_PHIX(9) ET_PHIX(9)*
FP1 21
FP1 22

X = 0 OR 1 depending on the cycle.

ET_OUT(19:0)

ET output to PreFRED.

Differential Drivers

FP2

U23 DS90C031 DIP
U24 DS90C031 DIP
U25 DS90C031 DIP
1A 2A 3A 4A G G NULL
1Y 1Z 2Y 2Z 3Y 3Z 4Y 4Z

FP2 TRIG(0) TRIG(0)*
FP2 TRIG(1) TRIG(1)*
FP2 TRIG(2) TRIG(2)*
FP2 TRIG(3) TRIG(3)*
FP2 TRIG(4) TRIG(4)*
FP2 TRIG(5) TRIG(5)*
FP2 TRIG(6) TRIG(6)*
FP2 TRIG(7) TRIG(7)*
FP2 TRIG(8) TRIG(8)*
FP2 TRIG(9) TRIG(9)*
$P
FP2 21
FP2 22

TRIG output to PreFRED.

TRIG_OUT(19:0)

VCC

CS_OUT(19:0)

9:0
19:10

CS_OUT(9:0) = TRIG_SUM_MUX(9:0)
CS_OUT(19:10) = ET_SUM_MUX(9:0)

ET_SUM_MUX(9:0)

TRIG_SUM_MUX(9:0)

EPROM disabled

Let there be light!

Octal buffers/ drivers with OC outputs

U58 SN74BCT760 DIP A1 A2 A3 A4 G NULL Y1 Y2 Y3 Y4

R16 240 1 2 red LED0 1 2

U56 SN74BCT760 DIP A1 A2 A3 A4 G NULL Y1 Y2 Y3 Y4

R3 240 yellow LED5 1 2
R10 240 yellow LED6 1 2
R11 240 red LED7 1 2
R12 240 yellow LED8 1 2
R17 240 green LED9 1 2

U31 T4HCT123 RC C A B CLR

R7 10k
C2 0.1uF

U30 T4HCT123

R8 100k
C3 0.1uF

U31 T4HCT123

R34 100k
C11 0.1uF

U56 SN74BCT760 DIP A1 A2 A3 A4 G NULL Y1 Y2 Y3 Y4

R13 240 red LED1 1 2
R14 240 green LED2 1 2
R15 240 yellow LED3 1 2
R18 240 green LED4 1 2

U30 T4HCT123

R6 100k
C1 0.1uF

Dual retriggerable monostable multivibrator with reset

Parity
Clock Error
Power (+5V)
L1_Rclk
VME_Select
Load
Run
Halt*

Lights(7:0)

Control(130:0)

Device 2 Device 1

U130 EPC1 DATA DCLK OE nCASC nCS NULL
U129 EPC1 DATA DCLK OE nCASC nCS NULL

Multiplexer U28 SN74CBT3257 DIP 1A 1B 2A 2B 3A 3B 4A 4B NULL 1Y 2Y 3Y 4Y -A/B G
R31 1K R30 1K R29 1K
R32 1K

FP4 DCLK
FP4 CONF_DONE
FP4 nCONFIG
FP4 nSTATUS
FP4 DATA0
FP4 ground
FP4 VCC
FP4 NC1
FP4 NC2
FP4 ground

R33 1K

FLEX_config(9:0)

FP4: connector to Bit Blaster Download Cable (PS mode)

R28 1K R27 1K R26 1K R25 1K

FP3 TDO
FP3 TMS
FP3 NC3
FP3 TDI
TCK
FP3 ground
FP3 VCC
FP3 NC4
FP3 NC5
FP3 ground

VME_config(9:0)

FP3: connector to VME_Interface Bit Blaster (JTAG mode)

The parity LED lights up when the even wedge ET summary is sent first.
Note that these signals are multiplexed in two sequential steps of 66 ns each.

DATE	REVISION DESCRIPTION
6 Mar 98	Made everything consistent with 10 lines of ET_OUT and TRIG_OUT. -NJL
8/15/98	put new symbols
31 Aug 98	Updated Lights signals. - NJL
May 28 99	Added monostabil on Lights(7)

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Crate Sum/FP

SHEET 19 OF 20
DATE 16 May 96
DRWN Dave Toback

C-2329
REV A