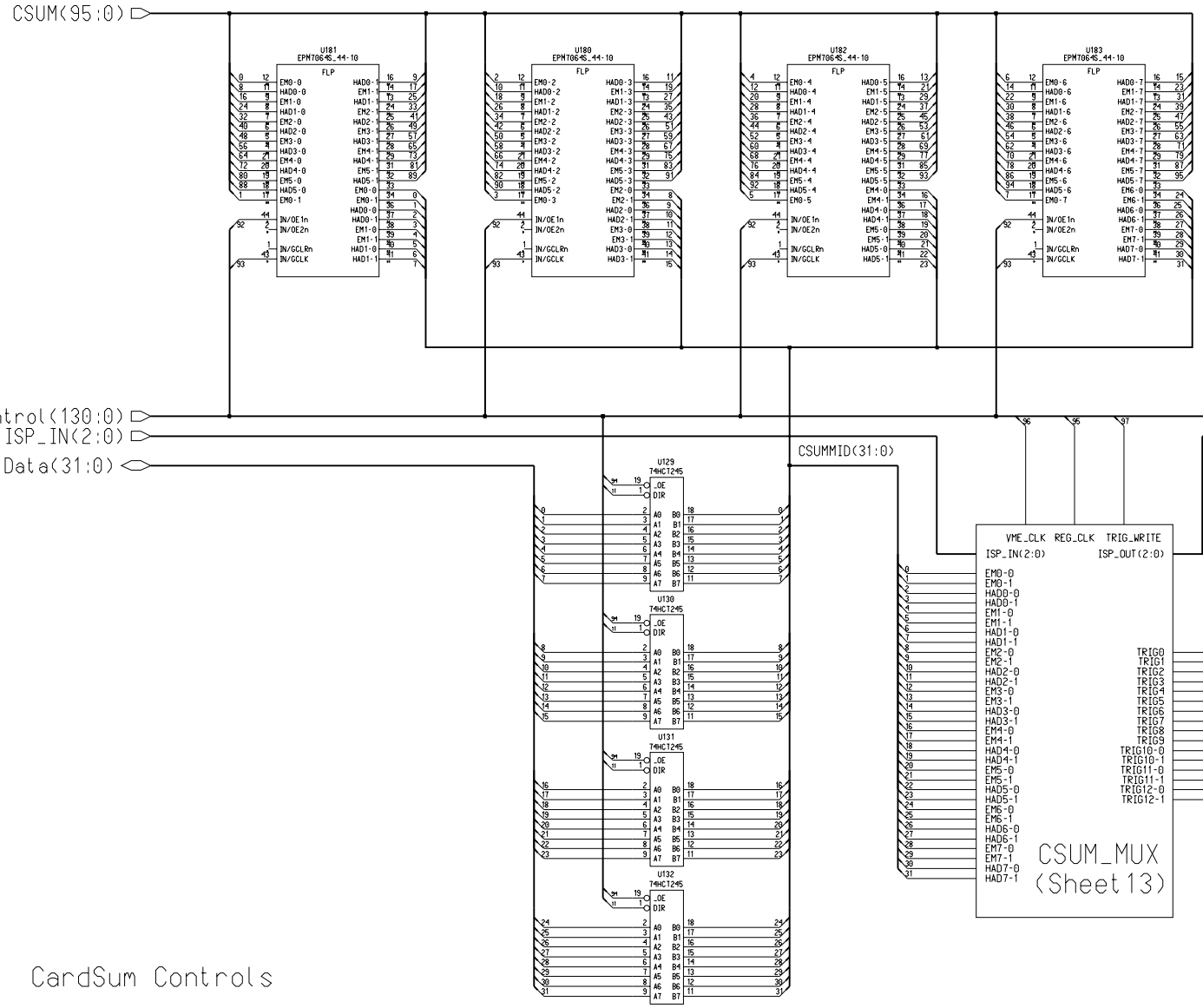
Bit	Bit	Bit	Bit	Bit	Bit	Bit	Bit
EM0	EM1	EM2	EM3	EM4	EM5	EM6	EM7
HAD0	HAD1	HAD2	HAD3	HAD4	HAD5	HAD6	HAD7

2 Bit Summers



Delay to go through the CSUM and CSUM_MUX chips = 18ns for CSUM + 31ns for CSUM_MUX + 15ns Buffer + Backplane (5ns) + Register on CS = 69ns + Register on CS out of 132ns. Thus there is no clocking done by HEART for CSUM_MUX

Buffers to Backplane

CardSum Controls

Control(92) - CardSum Output Enable*
Control(93) - Latch CardSum Mid
Control(94) - Enable VME Data Access*
Control(95) - Clock VME Data into MUX (Configuration)
Control(96) - Clock VME Data into MUX Registers (fake data)
Control(97) - Enable VME Read of Data in MUX
Control(98) - CardSum Output Enable*
Control(11) - Write

ISP INPUT
ISP_IN(0) - TDI From Previous Chip in Chain
ISP_IN(1) - TMS Signal
ISP_IN(2) - TCK Signal

ISP OUTPUT
ISP_OUT(0) - TDO To Next Chip in Chain
ISP_OUT(1) - TMS Signal(Tied to ISP_IN(1))
ISP_OUT(2) - TCK Signal(Tied to ISP_IN(2))

DATE	REVISION DESCRIPTION
26 June 1995	Second Prototype: Major changes to had and em triggers and MUX.
18 Nov 1996	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / CardSum

SHEET 12 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
REV C