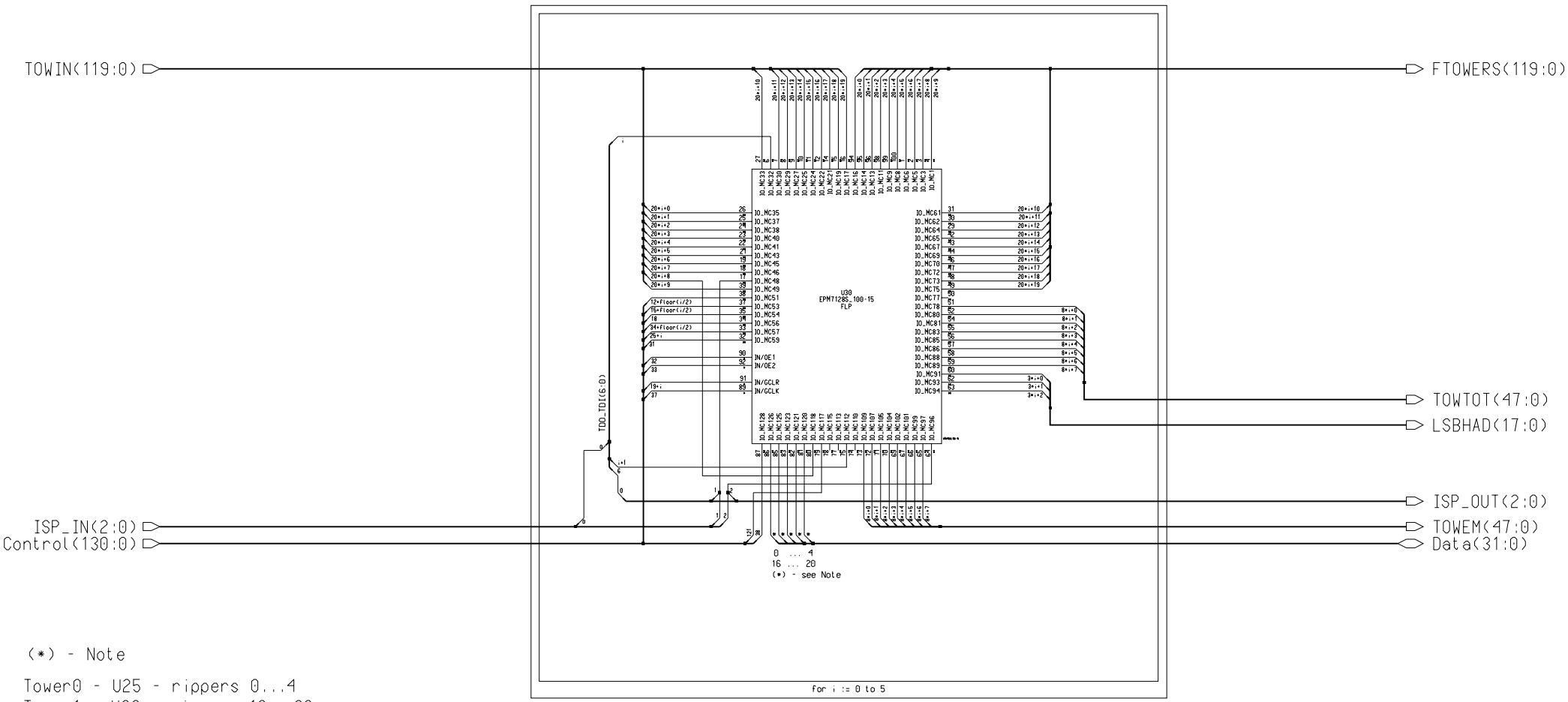
Control Signals

Control(14:12) - EM VME Clock
Control(17:15) - HAD VME Clock
Control(18) - Selector for the Had/Em Bits
Control(24:19) - EM Masking Bits
Control(30:25) - HAD Masking Bits
Control(31) - VME Data Select Bit 0
Control(32) - VME Data Select Bit 1
Control(121) - VME Data Select Bit 2
Control(33) - Enable Tower Data*
Control(36:34) - VME Select for Reading*
Control(37) - Tower Clock
Control(38) - Select for Energy Granularity

ISP INPUT
ISP_IN(0) - TDI From Previous Chip in Chain
ISP_IN(1) - TMS Signal
ISP_IN(2) - TCK Signal

ISP OUTPUT
ISP_OUT(0) - TDO To Next Chip in Chain
ISP_OUT(1) - TMS Signal(Tied to ISP_IN(1))
ISP_OUT(2) - TCK Signal(Tied to ISP_IN(2))



(*) - Note

Tower0 - U25 - rippers 0...4
Tower1 - U26 - rippers 16...20
Tower2 - U27 - rippers 0...4
Tower3 - U28 - rippers 16...20
Tower4 - U29 - rippers 0...4
Tower5 - U30 - rippers 16...20

TDO_TDI(6:0) Explanation

TDO_TDO(6:0) - This is the serial input and output for the 6 TOWLAT chips for ISP. The bus connects TDO of chip 0 to TDI of chip 1, TDO of chip 1 to TDI of chip 2, etc... Finally, bit 6(TDO of chip 5) is tied to ISP_OUT(0) to pass to the next chip in the chain.

DATE	REVISION DESCRIPTION
19 June 1995	Second Prototype: Major Changes to entire data path.
18 Nov 1996	3rd Prototype - Bug Fixes

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
DIRAC / TOWLAT

SHEET 15 OF 24
DATE 18 Nov 1996
DRWN JW

C-2351
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